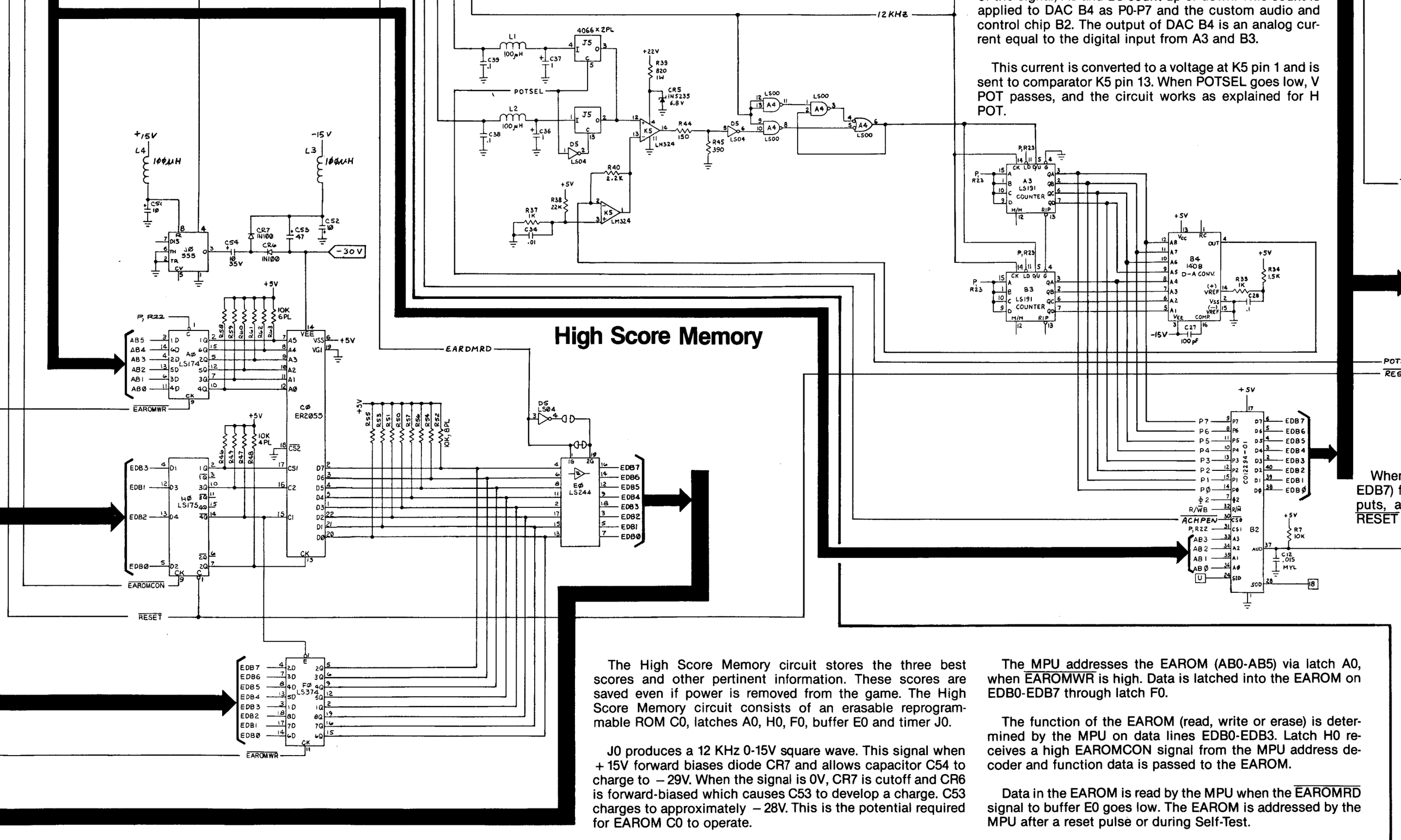
High Score Memory



The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM C0, latches A0, H0, F0, buffer E0 and timer J0.

J0 produces a 12 KHz 0-15V square wave. This signal when + 15V forward biases diode CR7 and allows capacitor C54 to charge to − 29V. When the signal is 0V, CR7 is cutoff and CR6 is forward-biased which causes C53 to develop a charge. C53 charges to approximately − 28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) via latch A0, when $\overline{\text{EAROMWR}}$ is high. Data is latched into the EAROM on EDB0-EDB7 through latch F0.

The function of the EAROM (read, write or erase) is determined by the MPU on data lines EDB0-EDB3. Latch H0 receives a high EAROMCON signal from the MPU address decoder and function data is passed to the EAROM.

Data in the EAROM is read by the MPU when the $\overline{\text{EAROMRD}}$ signal to buffer E0 goes low. The EAROM is addressed by the MPU after a reset pulse or during Self-Test.