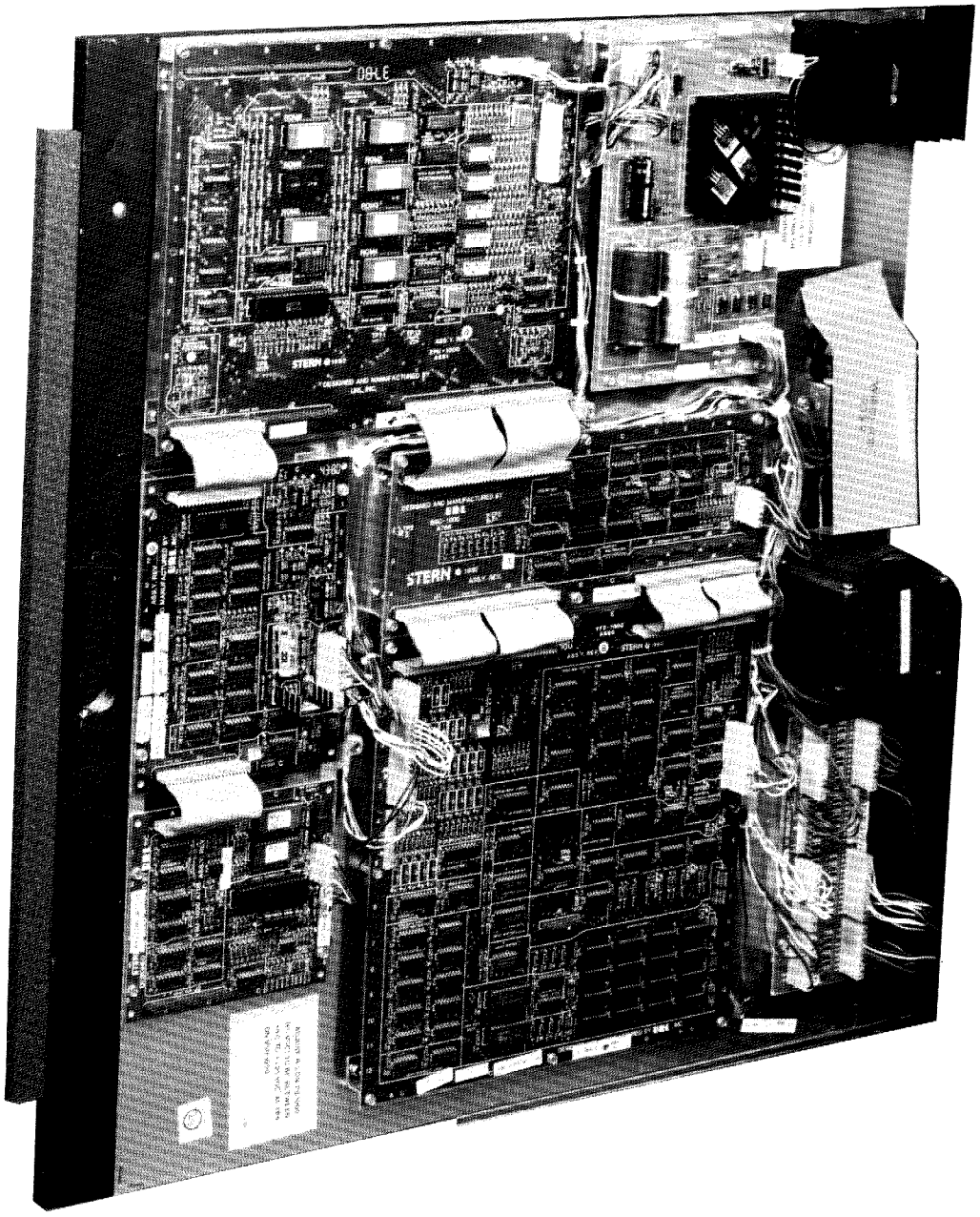
TECHNICAL MANUAL



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STERN VIDEO SYSTEM 1000

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SECTION I

INTRODUCTION AND REFERENCE DATA

1.1 INTRODUCTION

With respect for the job performed by the field Service Technician, Stern Electronics Inc., through its Electronic Research, Development and Manufacturing subsidiary, Universal Research Laboratories, Inc., pledged to provide all possible servicing and trouble shooting aids. Service concepts that have been in the discussion and planning stages are now a reality as indicated by the following features.

1) All the electronics are mounted on a front pull-out drawer which makes it possible to work on the circuit boards without moving the game away from the wall and while viewing the monitor in its normal position. Game controls and other switches are also accessible in the test position.

2) The system provides self test features: One is a flashing LED which cycles through eight circuit tests any time the system receives a reset signal. In addition to the LED flashes, an audible tone is provided with each flash.

3) The individual circuit boards of the system incorporate extensive silk screen labeling which identify not only the component parts but the functional circuits as well. In many cases, the circuit board is as easy to read as the schematic.

4) Switch circuits have been incorporated for disabling various feed back loops to eliminate automatic functions. Such functions make it difficult to analyze individual circuit problems.

5) An outstanding tool for the identification of components with reference to the schematic diagrams is a method of dividing the board into various mapped grid zones by letters and numbers. The designation of an integrated circuit (i.e. 4A, 6B, etc) is its location with reference to the grid zone. Any integrated circuit on the schematic can be located almost instantly on the board by the grid zone coordinates. Non-integrated components such as resistors, capacitors, diodes, switches and transistors are numbered in ascending order from left to right and top to bottom of the board.

6) A new troubleshooting system of decoding circuit information into "go" or "no go" indications is available. This system is called 'Signature Analysis" and does require some unique test equipment.

TABLE 1-1
GENERAL TECHNICAL DATA

FUNCTION	VALUE
Vertical sweep frequency	60 HZ
Vertical sweep time	16.666 milliseconds
Horizontal sweep time	64 microseconds
Total horizontal lines	262 (reduced by blanking signal)
Usable (displayable) horzontal lines	223
Total pixels (horizontal line time)	320 (64 usec/200 nanosecond clock)
Usable pixels per horizontal line	256
Usable bytes per horizontal line	32 (256 bits/8)
Usable pixels per field frame	57,088
Clock oscillator frequency	10 MHZ (crystal controlled)
CPU clock frequency	2.5 MHZ
System clock frequency	5.0 MHZ & 2.5 MHZ
Field rate	60 HZ (16.666 ms)
Frame rate	Same as field rate (non-interlaced)
Line voltage	Adjustable for 120 or 240 VAC.
Line frequency	50-60 HZ
Line current	Less than 2A @120 VAC line voltage (running)

TABLE 1-2

SYSTEM MEMORY MAP

CHIP REF.	HEX VALUE	BOARD	SPREAD	DATA BITS USED	FUNCTION
1C	0000-07FF	ZPU-1000	2K		PROGRAM PROM
1E	0800-09FF	ZPU-1000	1/2K	4,5,6,7	CMOS RAM WITH BATTERY BACK-up
2E	0800-0BFF	ZPU-1000	1K	0,1,2,3	SCRATCH-PAD RAM
1E	0A00-0BFF	ZPU-1000	1/2K	4,5,6,7	OPTIONAL CMOS RAM WITH BATTERY BACK UP
1D	1000-17FF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
3D	1800-1FFF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
4D	2000-27FF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
6D	2800-2FFF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
4C	3000-37FF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
3C	3800-3FFF	ZPU-1000	2K (2048)	0-7	PROGRAM PROM
	4000-43FF	VFB-1000	1K (1024)	0-7	SCRATCH PAD RAM
	4400-5FFF	VFB-1000	7K (7168)	0-7	SCREEN-IMAGE RAM
	6000-63FF	VFB-1000	1K (1024)	0-7	MAGIC SCRATCH-PAD RAM (SEE NOTE)
	6400-7FFF	VFB-1000	7K (7168)	0-7	MAGIC-IMAGE RAM (SEE NOTE)
	8000-87FF	BSC-1000	2K	0-7	COLOR LOOK-UP
	*	VSU-1000	4K	0-7	VOICE PROMS

NOTE:
The term "magic" refers to the Shifter/Flopper, ALU and MUX circuits that modify the video signal as it is written to the Screen Image RAM (See Fig. 3-6). Magic operations occur when address bit A13 is at logic level 1.

* not in the Z-80 address space

TABLE 1-3
ZPU-1000 I/O PORT DATA

PORT NO. (IN HEX)	NOTES	FUNCTION
40-5F		1/0 DECODE FOR OTHER BOARDS
60		SWITCHES: SW9-SW16 VIA Q9
61		SWITCHES SW1-SW8 VIA Q10
62		SWITCHES SW17-SW24 VIA Q7
63		SWITCHES SW25-SW32 VIA Q6
64		SWITCHES SW33-SW40 VIA Q8
65 &	USES DATA BIT D0	SWITCH S2 VIA Q4
65	USES DATA BIT D7	TEST SWITCH VIA Q11
66	RESETS FLIP FLOP 7G	ILLUMINATES LED CR 45
67	SET FLIP FLOP 7G	EXTINGUISHES LED CR 45

NOTE:
Port enabling is performed by decoder 7E as shown on Figure 3-4.

TABLE 1-4

VFB-1000 BOARD I/O PORT DATA

PORT NO. IN HEX	FUNCTION
	All following data based on IOADD* using ports 40 thru 5F as shown in Table for the ZPU-1000 Board I/O ports
48	SWITCH PORT 1 (CHIP 4D,2Y0 OUTPUT)
49	SWITCH PORT 2 (CHIP 4D,2Y1 OUTPUT)
4A	SWITCH PORT 3 (CHIP 4D,2Y2 OUTPUT)
4B	TO 8 BIT LATCH 6C (CHIP 4D,2Y3 OUTPUT)
4C	480 HZ NMI "ON" (INPUT OR OUTPUT)
4D	480 HZ NMI "OFF" (INPUT OR OUTPUT)
4E	INTERRUPT INPUT (MIDSCREEN/ENDSCREEN) ON BIT Ø, INTERRUPT RESET
	INTERCEPT INPUT ON BIT 7
4F	INTERRUPT ENABLE (OUTPUT TO BIT 0)

NOTE:
For I/O circuits refer to Fig. 3-6 and its references.

TABLE 1-5
SB-1000 BOARD I/O PORT DATA

PORT NO. (IN HEX) WITH W1 CONNECTED	PORT NO. (IN HEX) WITH W2 CONNECTED	FUNCTION AND/OR DATA
	All following data based on IOADD* using Port 40 thru 5F as shown in Table for the ZPU-1000	
40	50	Control register #3 if control register #2 bit Ø = Ø Control register #1 if control register #2 bit Ø = 1
41	51	Activates control register #2
42	52	Most significant-byte-buffer-register is enabled.
43	53	Timer NO.1 latches.
45	55	Timer NO.2 latches
46	56	Noise register, 2 bits if D7 = 0 and D6 = 0
46	56	Volume register, NO. 1, 3 bits if D7 = 0 and D6 = 1
46	56	Volume register, NO. 2, 3 bits if D7 = 1 and D6 = 0
46	56	Volume register, NO. 3, 3 bits if D7 = 1 and D6 = 1
47	57	Timer NO.3 latches.

NOTE:
Ports 40 thru 43, 45 and Port 47 address registers within the type-6840 programmable timer module.

TABLE 1-6

VSU-1000 I/O PORT DATA

PORT NO. (IN HEX) WITH W1 CONNECTED	PORT NO. (IN HEX) WITH W2 CONNECTED	BIT 7	BIT 6	FUNCTION
44	54	0	0	Word control output
44	54	0	1	Frequency & Volume control (output)
44	54			Feedback (input)

NOTES:

1. Volume is controlled by bits 3,4 & 5 of the frequency and volume control register. The frequency of the clock input to the voice chip is controlled by bits 0,1 and 2 of the register.

2. The frequency is per the following chart:

BIT: 2	1	0	FREQUENCY (kHz)
0	0	0	19.5
0	0	1	20.8
0	1	0	22.32
0	1	1	24
1	0	0	26
1	0	1	28.4
1	1	0	31.25
1	1	1	34.7

SECTION 2

SYSTEM OPERATION

2.1 OVERVIEW

The system block diagram of Figure 2-1 illustrates an important concept of video games as follows. In addition to the usual numerical operations performed by the microprocessor (Z-80), it also generates a unique 8-bit data signal which is a binary number and also a digital video signal. This 8 bit byte can modulate the CRT video circuits to produce a visual pattern. A high logic level bit (1) will produce a bright spot with color while a logic low level (0) will produce a dark spot. Thus, each byte can control 8 picture elements (pixels) on the screen.

The video path which starts at the Z-80, reaches the Screen RAM (VFB-1000 board) for storage and then goes through the 8 bit latch to the serializing register. The register shifts the bits out one at a time through the color gates to the CRT color circuits.

Screen RAM stores a sufficent quantity of bytes to provide control of every pixel on the CRT screen and the total bit pattern in RAM is an electrical reflection of the displayed game.

2.2 SYSTEM DESCRIPTION

2.2.1 Z-80 MICROPROCESSOR, PROM AND STATIC RAM

Microprocessor Z-80 generates all required signals in response to instructions and digital data received from the bank of Programmable Read only Memories (PROMs). THE PROMs have been programmed to store the binary codes for digital video image construction and the game actions.

In addition to the PROM's, two static RAM's are immediately associated with the Z-80 for "scratch-pad" memory during computations and for storage of important statistics such as: high score to date, number of coins deposited and the number of free games won. Battery standby-power is automatically applied to the RAM holding the statistics to avoid loss during a power-off condition.

2.2.2 Bus System and Signal Lines

NOTE

*Denotes a signal that is true (active) when it is at a logic zero level. This indication is used throughout this manual instead of the "over-bar" for the "not" indicator.

ADDRESS BUS

The System Address Bus is 16 bits wide and it is immediately buffered at the Z-80 output by tri-state line drivers. While these drivers are equipped for disabling (High-impedance state) by appropriate signals, they are never turned off in this system. In addition to the selection of a specific memory location, the lower 8 bits of the bus provide for enabling and disabling various circuits throughout the system (I/O ports). Examples of these special port addresses are shown by the lines extending to the Voice Synthesizer Board (VSU-1000) and the Sound Generation Board (SB-1000). I/O ports are listed in the Tables of section 1.

DATA BUS

The CPU data bus is an 8-bit wide bidirectional bus which connects directly to the outputs of the PROM and static RAM memories, but is buffered by tri-state bidirectional drivers before reaching the System Data Bus (and the other circuits). Any signals appearing on the System Data bus can be transferred to the CPU Bus and applied to the Z-80 by proper control signals applied to the tri-state drivers. The Data Bus is time shared (multiplexed) with a number of circuits and various types of information will appear on the bus at different times. The block diagram indicates the Time-sharing circuits are: Program PROMs, static RAM's, 40-setting-switches via chip 5E, game controls and coin door mechanism via chips 6A & 5B on the VFB-1000, and digital data from line drivers 6D which receive signals from the Screen RAM via two 4-bit latches 10D & 11D. The path through line drivers 6D is used only during a RAM read by the Z-80. Multiplexing of these signals is under software control (instructions) stored in the PROM's. When the Z-80 reaches a place in its program where information about the players game controls or the service switch settings is needed, it is instructed to send out an I/O port address for the appropriate circuit on the Address Bus. The addressed circuit responds by placing the information on the data bus which is then fed-back to the Z-80 and incorporated into the related computations.

2.2.3 CPU Reset Signal

A RESET* signal is generated by a the power-up reset circuit each time a power-up occurs. Also, a RESET button is provided on the ZPU-1000 board to allow service personnel to restart the game and cycle through the LED self tests. The RESET* signal restores all registers (counters, etc.) back to the initialization state of zero. Thus when the game starts, the first instruction in PROM memory will be requested (by the program counter in the Z-80) and all actions will start off at the proper point. The starting point is a self-test program. At completion of the program, the game is ready to play.

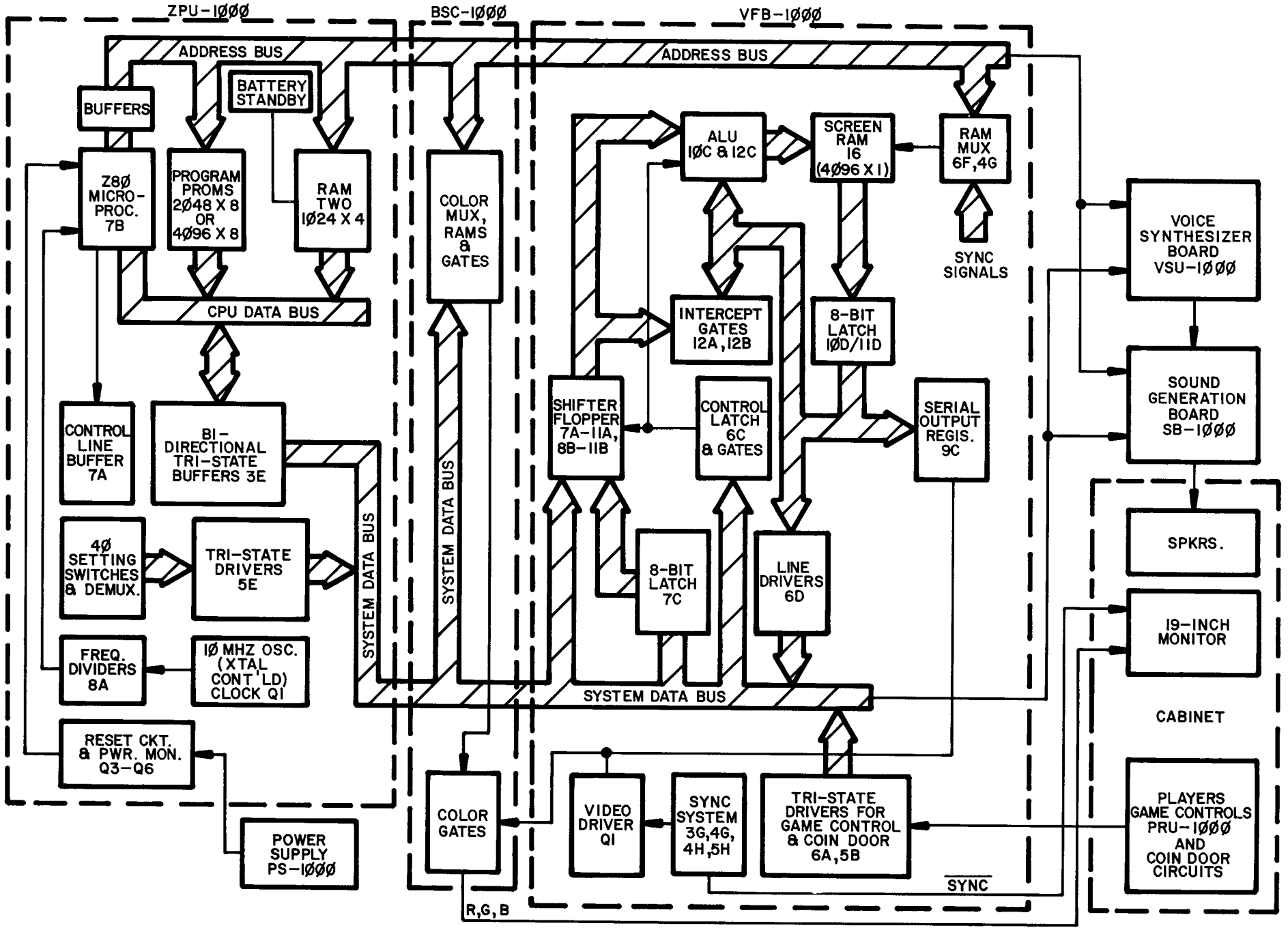


FIGURE 2-1 BLOCK DIAGRAM, SYSTEM

2.2.4 Clock Signals

A 10 MHz crystal controlled oscillator (on the ZPU-1000 Board) is divided down to provide a 5 MHz and a 2.5 MHz clock. The Z-80 uses only the 2.5 MHz clock which provides sequencing (timing) signals to the various registers and counters in the Z-80 itself and synchronizes the Z-80 with the other parts of the system.

2.2.5 Digital Video Path

The Z-80 assembles 8-bit Bytes each of which will represent a portion of the monitor picture to be displayed. There are 32 bytes per each horizontal line. Each byte is assembled by the Z-80 as directed by the PROM instructions and then transferred out the CPU Data Bus, through the bidirectional buffers and onto the system Data bus. The signal is routed through the bus of the BSC-1000 color board and then into the VFB-1000 board. The bus path through the BSC-1000 color board is merely a matter of mechanical expediency relative to the board location in the system since no priority or protocol bus positions exist. Any position along the system bus is equivalent to every other position. The bus data is gated into the appropriate circuits by either an address decoder scheme or a port read/write circuit. The BSC-1000 color board is activated by a different address than the VFB-1000 board and is inactive during the Z-80 video memory write cycle.

2.2.6 Shifter Flopper Circuits

At the VFB-1000 board, the video byte is applied to the shifter/flopper through two paths, one of which includes 8 bit latch chip 7C. The latch stores the byte until the next write cycle occurs at which time both signals are mixed at the input to the shifter/flopper. This process restores a bit deleting action inherent in the circuits and is described in Section 3.

Figure 2-1 shows a third path from the System Data Bus leading to "control latch 6C and gates". This path operates only during a port write from the Z-80 and will store an 8-bit byte in the latch. This byte is constructed as an 8-bit control code rather than a video type signal. The port-write control byte is latched-in prior to the the video signal. The control byte will instruct the shifter/flopper circuits and the ALU (Arithmetic Logic Unit) circuit how they are to modify the video byte.

Basically, the modifications that the shifter/flopper can produce are: (1) A rearrangement of the bits so as to move specific bits upward (toward the MSB) or downward (toward the LSB) which, in turn, will visually move the data on the screen or, (2) Completely reverse the bits (flop action) so as to visually reverse the image.

For a non-changing display (scene), the status (1 or 0) of every RAM data bit would remain unchanged. The illusion of movement is created by changing the status of the bits in a specific, orderly manner. For example, a single bright spot (pixel) at the center of the screen would appear to move toward the right by sequentially changing the status of the next (later in time) pixel to a 1 while changing the present pixel to a zero. This is the electrical equivalent of moving the status bit sequentially through all the bits of a specific horizontal line. It will produce an equivalent visual movement. A left-hand movement requires that the bits preceeding the presently active bit be changed sequentially. An upward movement requires that equivalently-located bits on the preceeding horizontal line be changed, while a downward movement requires a change in the equivalently located bits on the following horizontal line.

2.2.7 Screen RAM and Serialization shifter

Screen RAM consists of sixteen 4096 x 1 bit chips organized into two separate systems of 4096 x 8 bits each. The two systems are operated in parallel with alternate addressing to provide a total Screen RAM of 8192 x 8 bits (8K Bytes) or 65,536 x 1 (65K) total memory bits.

The video flow path continues from the output of the Screen RAM to the 8 bit video latch (chips 10D and 11D). The byte will be transferred to the parallel-to-serial register (9C) which will apply the bits one at a time (at the 5 MHz clock frequency) through two parallel video paths to the CRT: (1) video driver Q1 for composite black/white and (2) the BSC-1000 color board for the RGB color signal. By the time the entire 8 bits have been shifted out, another byte will have been transferred from the Screen RAM to the data latch for a repeat of the action. This action will continue so as to apply 32 Bytes to each of the 223 usable horizontal sweep lines.

2.2.8 ALU and Intercept Circuit

ALU

The ALU has two inputs: one from the Shifter/Flopper video path and a second from the output of the two 4-bit latches (10D and 11D). Thus, the ALU can compare and logically combine new, incoming data bytes with already present data bytes existing in RAM. The logic function to be performed on the two signals is determined by the control code applied to the ALU from control latch 6C. One of the available logic functions is an exclusive OR that can be applied to the two signals. In this operation, only signals that have different logic states (1 and 0) will be passed by the ALU. Thus, if a video byte is compared against itself the resultant output is zero, or total electronic erasure of that byte. Other operations are described in Section 3.

Intercept Gates

The intercept gates (12A and 12B) have the same two input paths as the ALU described previously. Thus, the eight NAND gates will compare a previous video byte being fed into the ALU with a new byte just leaving the Shifter/Flopper circuits. The two bytes are compared bit-by-bit by the eight NAND gates so as to detect two corresponnding bits that have a logic 1. This indicates that two images are electrically becoming coincident with each other and will be displayed as one object overwriting another object on the screen. The intercept gate generates an output which is fed back to the Z-80 to alert it to the condition. The Z-80, as directed by the PROM software, then provides appropriate signals to change the game as required.

SECTION 3

DETAILED CIRCUIT DESCRIPTIONS

3.1 ZENTRAL PROCESSING BOARD (ZPU-1000) CIRCUITS

The Z-80 CPU (chip 7B, Fig. 3-1) is a complete microprocessor packaged in a 40 pin DIP chip which operates from a single power supply voltage of +5 Volts. The chip also requires a clock input signal to synchronize the internal circuits. The Z-80 pin functions and waveforms are provided in this section.

The clock frequency is 2.5 MHz obtained by dividing a 10 MHz crystal controlled oscillator by four, through two flip flops (chip 8A). The 2.5 MHz signal leaves the board and is used by other circuits of the system. A 5 MHz signal obtained from one of the two flip flop dividers is passed through AND gate 3A and also leaves the board.

There are three categories of Z-80 signals: (1) 16 address bits (A0-A15) which use the address bus, (2) 8 data bits (D0-D7) which use the data bus and (3) 13 control signals which essentially have independent conductors. The address bus uses two separate buffer chips 6B and 7D. In the case of the data bit signals, no buffer exists between the Z-80, the PROM and the two RAM memory chips and this bus is called the Z-80 Bus. The bus is buffered by 8 tri-state, bi-directional bus drivers in chip 3E (type LS245) prior to leaving the board. The direction of the data flow through chip 3E is determined by the logic state of the signal applied to its "direction" pin. A logic zero allows flow from the Z-80 to the system bus while a logic 1 provides an opposite flow path. The Enable pin (19) is grounded and the path is thus always operable in one direction or the other. The aforementioned "direction" pin will be logic 1 (data flow into the Z-80) only during the following conditions:

1. When the Z-80 reads memory addresses 4000_H through $FFFF_H$.
2. The time span of an interrupt acknowledge.
3. The time span of an I/O port read.

NOTE

* Denotes a signal that is true (active) when it is at a logic zero level. This indicator is used throughout this manual instead of the "over-bar" for the "not" indicator.

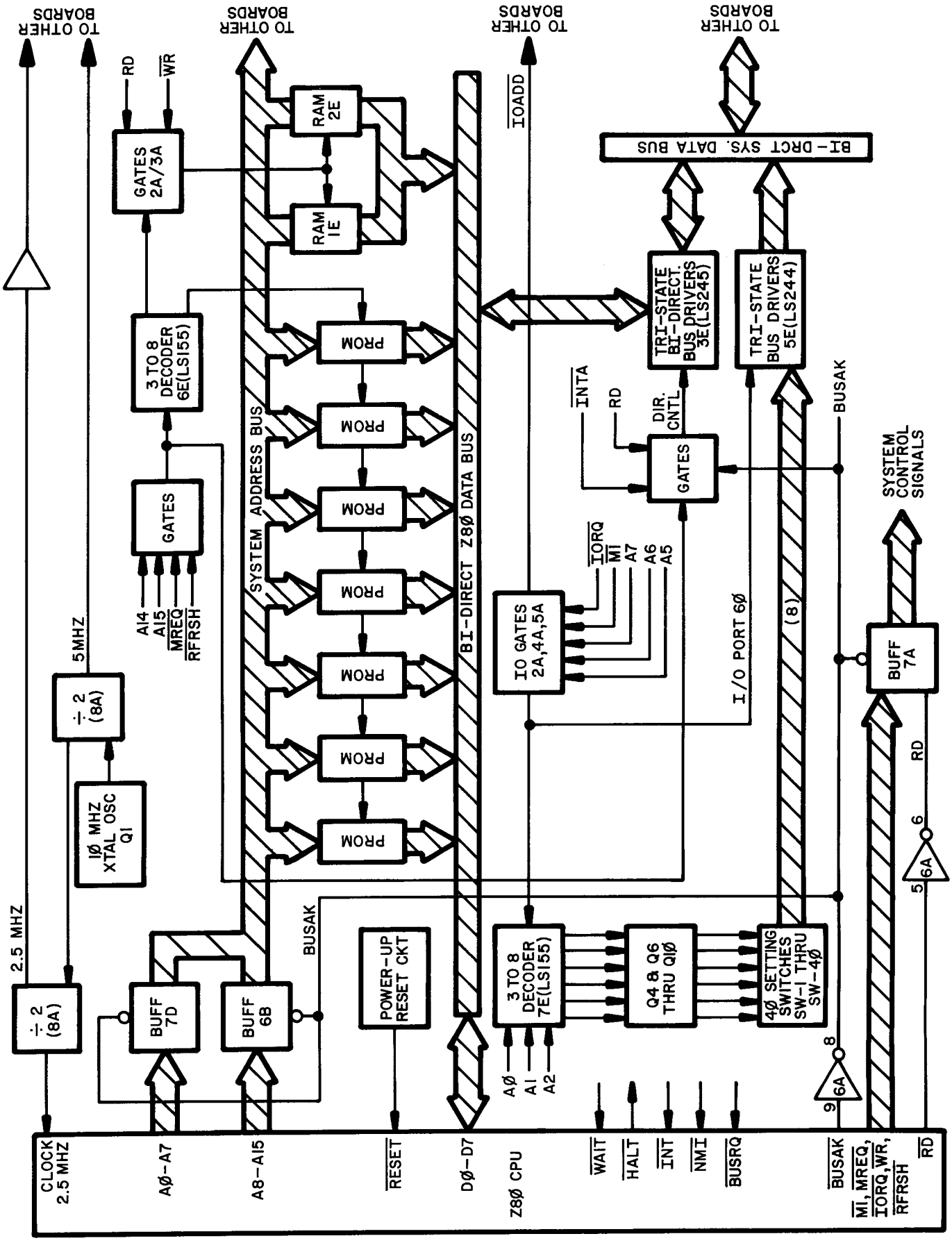


FIGURE 3-1 BLOCK DIAGRAM, ZPU-1ØØØ BOARD

TABLE 3-1

PIN FUNCTIONS FOR Z-80 MICROPROCESSOR

AO-A15 (ADDRESS BUS)

Tri-state output, active high. A sixteen pin bus used by the Z-80 to address or select specified device-RAM, ROM or I/O port. I/O addresses use the 8 lower bits.

DO - D7 (DATA BUS)

Tri-state input/output, active high. Used to convey information between the Z-80 and other devices. It is bidirectional and data flows both to and away from the Z-80.

CLOCK (PHI SYMBOL)

2.5 MHz input used by the processor to time internal events. Everything occurs in multiples of the basic clock cycle. The amount of time required to execute a given instruction depends on the instruction type. Times from 3 to 21 clock cycles can be expected.

HALT* (HALT STATE)

An Output: This pin will go low when a Halt instruction is executed by the processor. All functions stop. The only way to get out of a Halt is to RESET*,to interrupt, or use the non-maskable interrupt. HALT is not used in this system.

M1* (MACHINE CYCLE ONE)

Output, active low. Signifies that the processor is doing an OP-CODE Fetch,as opposed to a data read or write. Also occurs during IORQ* to signify the acknowledgement of an interrupt request.

WAIT*

Input, active low. Upon receiving a WAIT* signal, the processor holds the data, address and control lines as in the previous state for an extra clock cycle. If WAIT* is again true on the next clock cycle, the CPU again goes into a hold condition. If the WAIT* line is false, the CPU completes its instruction. For example, this feature is used to hold the CPU if it attempts to access the video RAM during a video cycle.

TABLE 3-1

PIN FUNCTIONS FOR Z-80 MICROPROCESSOR (CONT'D)

BUSRQ* (BUS REQUEST)

Not used in this system. Its normal purpose is to signify that an external processor is going to take command of the bus. The Z-80 responds by completing the instruction in process, turning off its data, address and control busses and bringing its BUSAK* (Bus Acknowledge) signal true. This condition is held until BUSRQ* is brought false.

NMI* (NON-MASKABLE INTERRUPT)

Input, negative edge triggered. Causes the processor to interrupt its normal program flow to respond to some special condition. Non-Maskable means that the Z-80 cannot ignore it.

RESET*

Input, active low. Resets the Z-80 so it is in a known condition after power-up. Upon RESET* going false (HI), the Z-80 will begin fetching instructions from address 0000_H, in hexdecimal (base 16).

INT* (INTERRUPT REQUEST)

Input, active low. Signifies that something important is occuring. Upon receiving it, the CPU alters its instruction execution to service the interrupt. Interrupts occur at the middle of, and at the end of, the video screen. It should be noted that the interrupt is maskable, and can be ignored under software control. When the processor responds to an interrupt, it brings both its IORQ* and M1* lines true simultaneously.

BUSAK* (BUS ACKNOWLEDGE)

Not used in this system. In other systems the Bus Acknowledge (output) is brought true LO in response to a BUSRQ* true signal.

RFSH* (REFRESH)

This output signal is brought true (LO) occasionally to assist in the refreshing of dynamic memories. When it occurs, MREQ* is also brought true. It is used only to insure that a CPU RAM cycle is a valid one, and not a refresh.

MREQ* (MEMORY REQUEST)

Tri-state output, active low. Signifies that a memory access is being made.

TABLE 3-1

PIN FUNCTIONS FOR Z-80 MICROPROCESSOR (CONT'D)

IORQ* (INPUT/OUTPUT REQUEST)

Tri-state output, active low. The output (Input/Output Request) signifies that a peripheral access is being made.

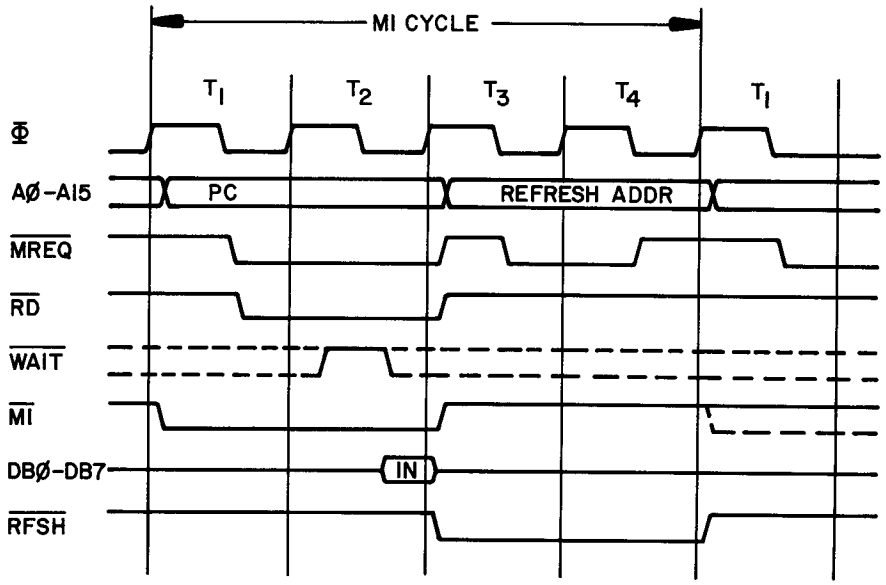
WR* (WRITE)

Tri-state output, active low when the Z-80 writes data.

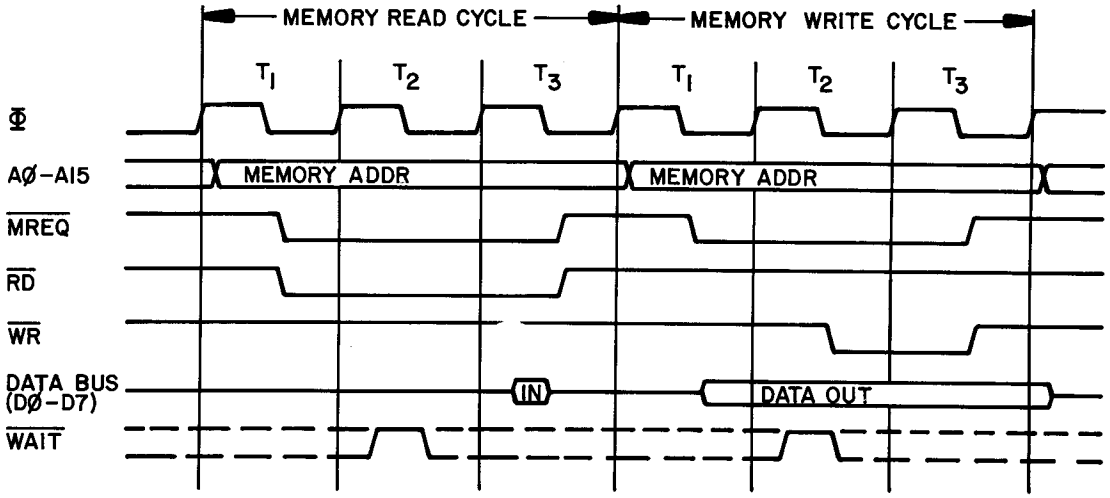
RD* (READ)

Tri-state output, active low when the Z-80 reads data.

* Indicates a signal which is true when at a logical zero.



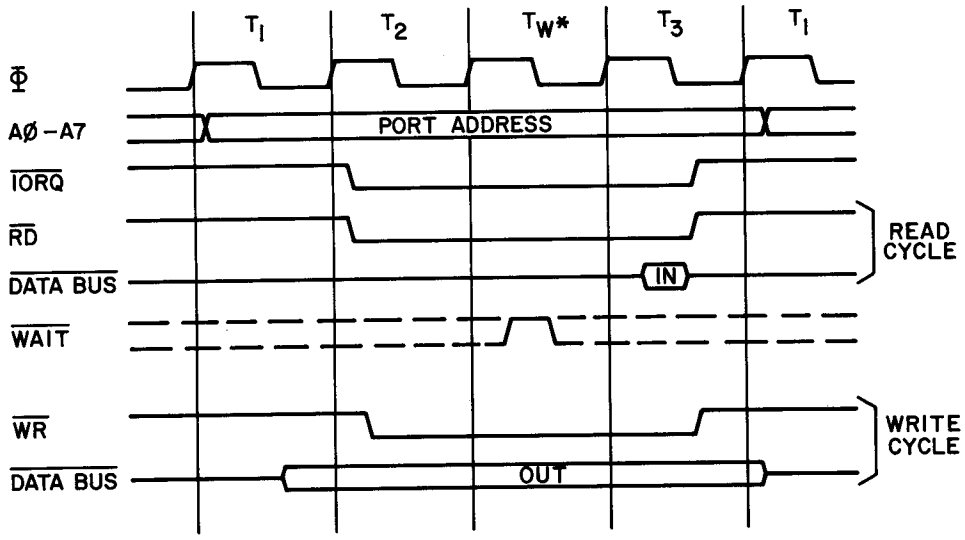
INSTRUCTION OP CODE FETCH



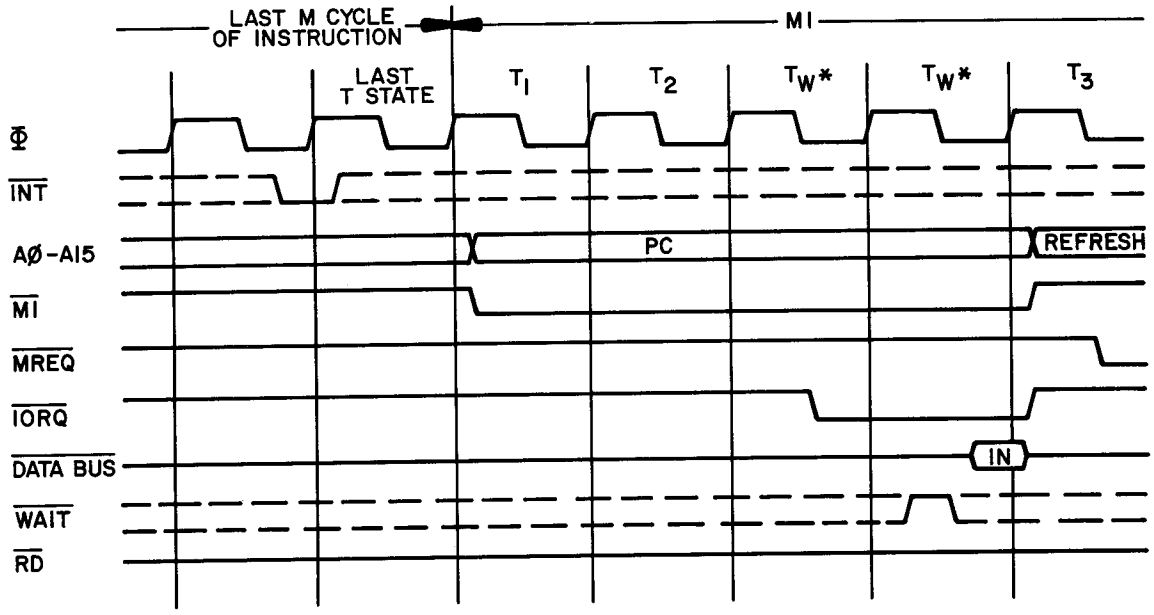
MEMORY READ OR WRITE CYCLES

NOTE:
A LOGIC ZERO $\overline{\text{WAIT}}$ SIGNAL WILL CAUSE THE ASSOCIATED T STATE TO BE REPEATED SO AS TO LENGTHEN THE ENTIRE GROUP.

FIGURE 3-2A Z80 TIMING WAVEFORMS



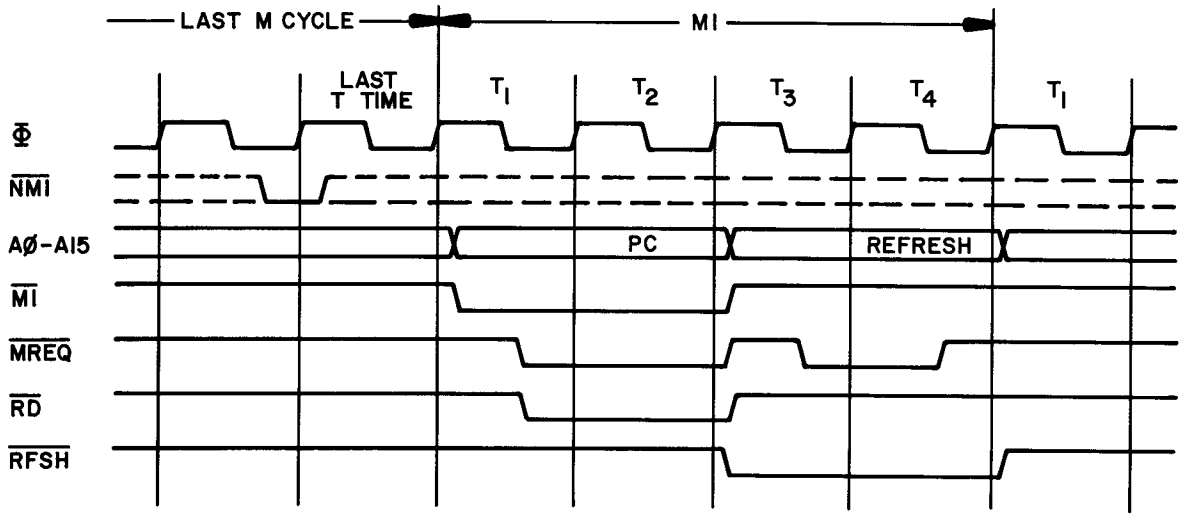
PORT INPUT OR OUTPUT CYCLES



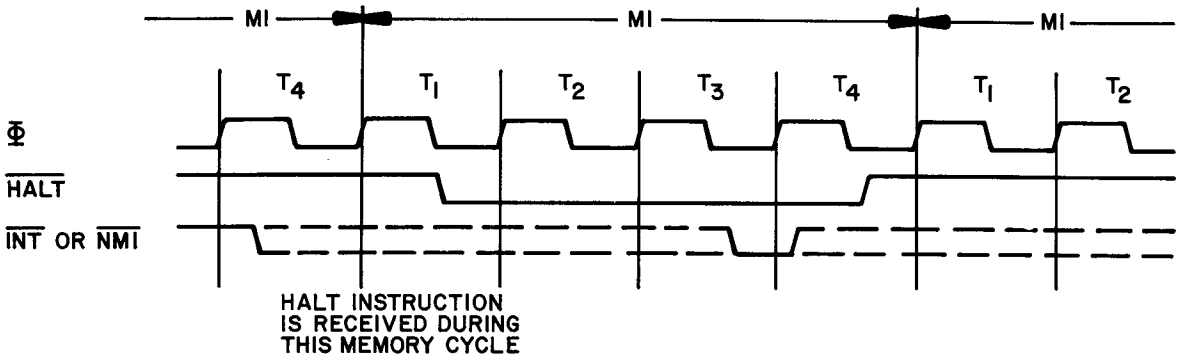
INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

NOTE:
A LOGIC ZERO WAIT SIGNAL WILL CAUSE THE ASSOCIATED T STATE TO BE REPEATED SO AS TO LENGTHEN THE ENTIRE GROUP.

FIGURE 3-2B Z8Ø TIMING WAVEFORMS



NON-MASKABLE INTERRUPT REQUEST OPERATION



HALT EXIT

FIGURE 3-2C Z8Ø TIMING WAVEFORMS

Discounting the clock input, there are thirteen control signals for the Z-80 . Six of these are buffered outputs via chip 7A (LS367). The Z-80 BUSAK* signal (which is logic 1 when not active) is inverted and applied as a permanent logic zero enabling signal to all bus buffers. Refer to table 3-1 for data.

There are five basic categories of Z-80 control functions (Figure 3-2) and they are: (1) Fetch, (2) Port Read,(3) Port Write, (4) Memory Read and, (5) Memory write. For one of the actions to occur, the entire combination of signals shown in that group (except for Wait*) will be generated by the Z-80 and appear on the appropriate channel conductors.

3.1.1 DECODER 6E, PROMS AND OP-CODE FETCH (M1 CYCLE) (Figure 3-3)

A fetch is the first machine cycle (M1) of any instruction and is addressed by the Program Counter (PC) in the Z-80 (which is started at zero each time the RESET* signal is received). The fetch waveform shows that the address contained in the PC is placed on the bus at the beginning of the M1 cycle. After reset, the address will be the first ROM memory location (0000). The address plus the Fetch control signals are applied to the circuits of Figure 3-3 and cause the following actions. Gating consisting of NOR gate 5A, inverter 6H and NAND gate 4A combine A14, A15, MREQ*, RFSH* and MEMDIS* such that pin 6 (output) of NAND GATE 4A will go to logic level 0 when A14 = A15 =MREQ* = 0, and RFSH* = MEMDIS* = 1. Under all other conditions the output of NAND gate 4A (pin 6) will be a logic 1.

DECODER CHIP 6E ACTION

Refer to Appendix A for the truth table of decoder chip 6E. The table indicates that only one output will go to logic level 0 for a specific set of binary input codes. This zero output line forms the chip select (output enable: OE*) for the PROMs and CE* for the scratch pad RAM via NOR gate 2A. See Figure 3-3.

PROM ENABLING

When two ROM chips are simultaneously enabled by the decoder, an additional method of electrically separating the chips is required. This separation is accomplished by bit A11 at pin 18 (chip enable*) which is inverted through inverter 8G and applied to the twin of each group. Thus, if chips 1D and 3D have been selected by line 2Y1* of decoder 6E, chip 1D will be enabled only when bit A11 is logic 0: chip 3D will be enabled only when bit A11 is logic 1.

PROM ADDRESSING

An enabled PROM reacts to the address bits A0-A10 applied to input address pins 1 thru 8 plus 22 and 23 (not shown on the block diagram) by outputting the data bits stored at the address. When the system first starts up after a reset, the first address requested by the Z-80 will be 0000 in PROM 1C.

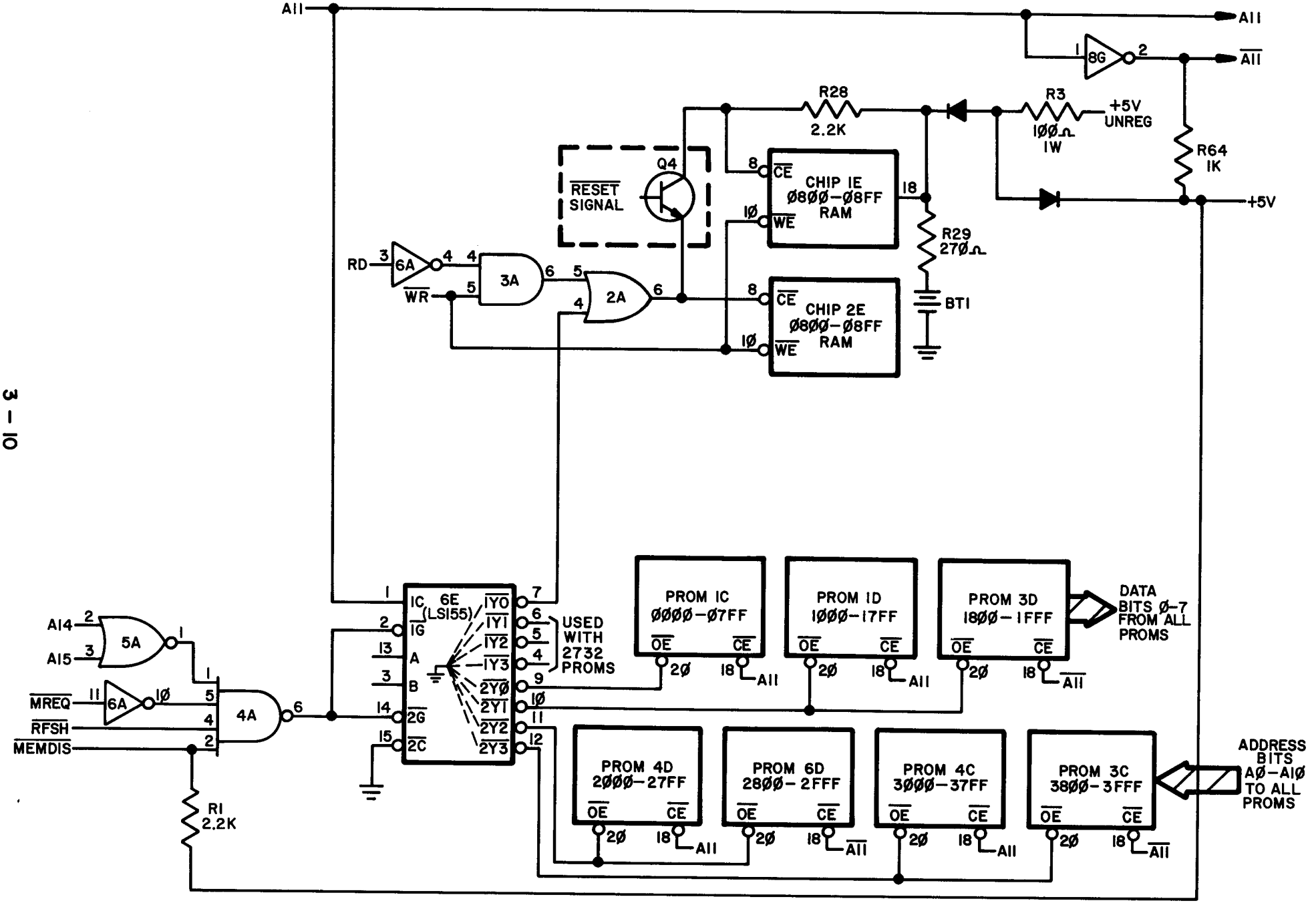


FIGURE 3-3 BLOCK DIAGRAM, DECODER 6E FOR ROM/RAM

The Z-80 uses its T3 and T4 clock cycle times to decode and execute the fetched instruction and no other operations can occur except for a RAM refresh action. This refresh is not utilized.

3.1.2 DECODER 6E AND RAM CHIPS 1E/2E (Figure 3-3)

Chips 1E and 2E are used for Z-80 "scratch pad" memory when required. Also, chip 1E specifically stores all bookeeping information such as the high score, number of credits, etc. To avoid loss of this data during a power off condition, chip 1E receives back-up power from battery BT1. The battery is continuously trickle-charged when power is normal.

The Z-80 can read from the 1E/2E RAM under the conditions that the CE* (chip enable) pins (8) are at logic L0 and the WE* (write enable) pins (10) remain HI. To obtain a L0 at the CE* pin of chip 2E, the output (pin 6) of OR gate 2A must be L0. This requires both inputs of 2A to be L0.

For pin 4 of OR gate 2A to be L0 (as received from chip 6E), the 1G*/2G* enable pins of chip 6E must be receiving a L0 from NAND gate 4A. This requires the same set of inputs to 4A as for the Fetch (i.e. A14-L0, A15-L0, MREQ*-L0, RFSH*-HI) and will exist during a memory read cycle (Fig. 3-2). In addition, bit A11 into the 1C pin (pin 1) of chip 6E must be HI and the binary code from bits A12 and A13 (at pins 13 and 3, respectively) must be 00 (i.e. A=0 & B=0).

For pin 5 of gate 2A to be L0 (as received from AND gate 3A (pin 6), AND gate 3A must receive at least one L0 input. The required L0 is at pin 4 and occurs because the RD signal is an inverted version of the RD* Z-80 output (See inverter 6A, pins 5 and 6 on schematic diagram). During a READ cycle, the WR* signal line remains HI and is applied to pin 5 of AND gate 3A as well as to both RAM chips at pin 10 (WE*). AND gate 3A (pins 4,5 & 6) generates a zero going edge which then results in the RAM CE* line going to logic 0. This is necessary because the RAM requires that addresses be stable before a CE* active transition occurs. Gating the RD and WR* signals together in chips 6A (pins 3 & 4) and 3A (pins 4,5 & 6) satisfies this requirement.

The method of obtaining a L0 for the CE* pin of chip 2E has been covered. The L0 for the CE* pin of chip 1E is obtained through transistor Q2 in the following manner. The base of Q2 is normally at a positive voltage (except during a reset or a power-down) and the transistor will conduct when the output (pin 6) of OR gate 2A is logic L0 (the emitter of Q2 is tied to pin 6 of OR gate 2A). Conduction of Q2 causes a voltage drop across resistor R28 (2.2K) so the CE* pin (8) of chip 1E follows the logic L0 at the CE* pin of chip 2E.

Conduction of Q2 is prevented during a reset cycle, or a power-down, since the base voltage drops to zero during either condition. Without conduction through Q2, the CE* pin (8) of RAM chip 1E cannot drop and the chip remains disabled. This prevents

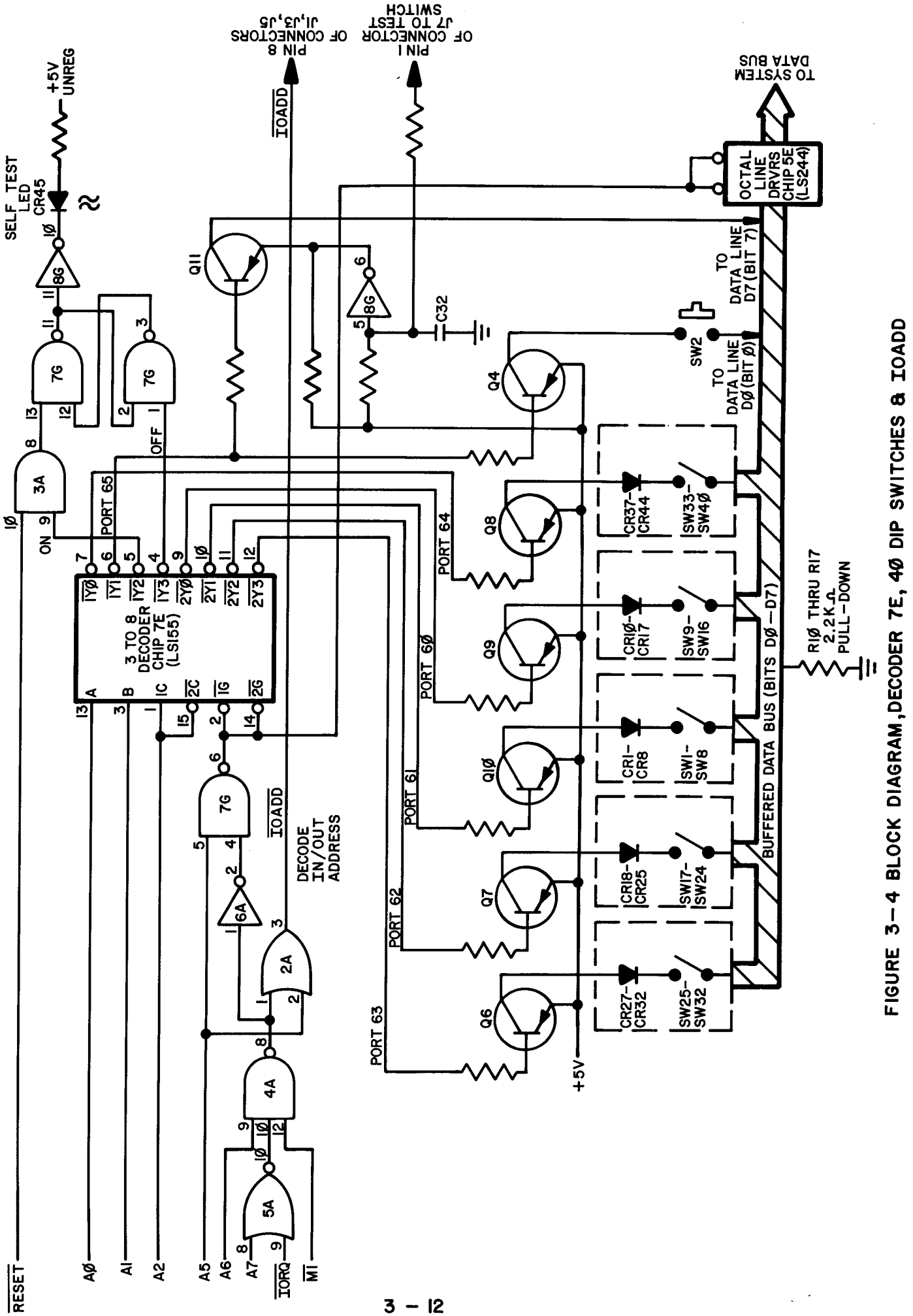


FIGURE 3-4 BLOCK DIAGRAM, DECODER 7E, 4Ø DIP SWITCHES & IOADD

any spurious signals generated during the reset operation from affecting the data stored in RAM 1E.

NOTE:

Any one of three memory chips may be contained in socket 1E. Jumpers W5, W6 and W11 determine which chips are used. Only one of the three jumpers will be used at any time.

CHIP	STERN PART NUMBER	USE JUMPER
6513 H	56A-6-S004	W5
6513 L	56A-6-S003	W6
6514	56A-6-S002	W11

3.1.3 DECODER 7E, 40 SETTING SWITCHES & IOADD* (Figure 3-4)

The 3-to-8 decoder chip (7E) in conjunction with the 3 gates 4A, 5A, and 7G which feed its 1G* and 2G* input pins (See Fig. 3-4) constitutes a Port decoder and will utilize the Z-80 I/O Port waveforms shown in Figure 3-2B.

Enable pins 1G*/2G* of chip 7E will be logic zero if NAND gate 7G has two HI (Logic 1) inputs. Tracing backwards from these two inputs indicates the following requirements: A5-HI, A6-HI, A7-L0, IORQ*-L0 AND M1*-HI. The L0 IORQ* along with the HI MI* condition is correct for an I/O port read or write (Fig. 3-2B). The Logic HI A5 and A6 bits constitute the Port address which is 60_H. This port address 60_H is then added to the binary codes applied to chip 7E (by bits A0, A1 and A2) to produce the complete port address.

The specific (1-of-8) output lead that is grounded will provide base current to the associated transistor causing it to conduct (i.e. line 2Y0* enables Q9, 2Y1* enables Q10, etc.).

Conduction of one of the five transistors (Q6 thru Q10) applies +5V to the associated eight diodes and eight switches in its collector path. Any switch in this collector path that has been manually turned ON will apply the +5 volts to the specific data bus line (D0 thru D8) to which it is connected. Since the Z-80 will enable only one of the five transistors at a specific time. It can "read" the condition of the eight switch groups at eight different time intervals (Port cycles) and identify the condition of every switch.

Each time a group of eight switches is enabled, the conditions of the eight data bus lines (HI for switch ON and LO for switch OFF) must be fed back to the Z-80 (a port read) so the settings can be utilized in the computations. The first part of this feed-back path is through chip 5E (line drivers shown in Fig. 3-1) which is enabled by the same logic LO of the port address (60_H) applied to the decoder. When enabled, chip 5E connects the 8 data lines to the system data bus.

The second part of the switch read (feedback path) is from the system data bus through the bi-directional drivers in chip 3E (Fig. 3-1), through the Z-80 data bus and into the Z-80.

3.1.4 DECODER 7E, SELF TEST LED AND FLIP FLOP 7G (Fig. 3-4)

The function of turning the self-test LED (CR45) ON and OFF is performed by decoder 7E using I/O PORTS 66 (pin 5: 1Y2*) and 67 (pin 4: 1Y3*). When the Z-80 is not controlling decoder 7E, both the 1Y2* and 1Y3* outputs will be logic HI. The 1Y2* output applies a HI to pin 9 of AND gate 3A. Pin 10 of AND gate 3A receives a logic LO RESET* when the power is first turned ON or when the RESET button is pressed. This LO input gives a LO 3A output (pin 8) which sets the flip flop so pin 11 is HI. This HI is inverted by 8G which applies a LO to the LED. The LED is turned ON (illuminated) by the voltage difference. The LED will also be turned ON by a LO from chip 7E at output 1Y2* (PORT address 66).

The Z-80 can turn the LED OFF (extinguish) by PORT writing address 67 which makes the 1Y3* output of chip 7E go LO. This reverses the flip flop and applies a HI to the LED via inverter 8G. With a high potential at both ends, the LED cannot illuminate.

3.1.5 POWER TEST AND RESET (See Schematic Diagram)

Start-up of the Z-80 is accomplished by a RESET* signal generated in the voltage monitor circuits consisting of transistors Q1, Q3, Q5 and associated components (Refer to Schematic of the ZPU-1000 Board). Transistor Q1 operates as a voltage comparator which receives an RC delayed voltage rise at its base. When the applied voltage level reaches a value sufficient to break down the Zener in its emitter, a voltage level will be applied to the base of transistor Q5 turning it ON. Transistors Q5 and Q3 function as a Schmitt Trigger and generate a sharp, steep sided level change to be applied through diode CR46 to NAND gate 7G at pin 9. If the power supply voltage has reached a sufficient positive value to enable pin 10 of NAND gate 7G, the gate will then output a logic zero at pin 8 which is inverted to a logic 1 through inverter 8G and applied to the RESET* pin of the Z-80. This rising, logic one signal now permits Z-80 execution of instructions.

Battery BT1 is constantly trickle charged through the 270 OHM resistor (R29) when power is normal. During a power loss, BT1 supplies power through R29 to the Vcc pin (18) of RAM chip 1E to avoid loss of its bookeeping data.

3.2 VIDEO FRAME BUFFER BOARD (VFB-1000) CIRCUITS

The majority of the VFB-1000 circuits can be grouped together into the "video group". This group handles the digital video data for CRT display and was described in a general manner in Section II (Digital Video Path).

3.2.1 VIDEO GROUP CIRCUITS (DETAILED) (Figures 3-5 thru 3-8)

Two separate functions are required of the Z-80 with respect to the video circuits: (1) generation of a video byte using data bits D0-D7, and (2) generation of control signals for these circuits. The control signals use the same data bits (D0-D7) applied to the same bus (System Data Bus) but are applied as an I/O cycle which will precede the video data. The control circuit path will be described first (paragraph 3.2.1.1) and the video circuit path will follow (paragraph 3.2.1.2).

3.2.1.1 CONTROL CIRCUIT PATH for the VIDEO GROUP

Control Latch 6C Action (Figure 3-6)

Latch 6C will store the 8-bit control code signals (D0 thru D7) put on the data bus by the Z-80 during an I/O cycle. The 8-bit control code is latched-in (clocked) and appears at the output of 6C on the rising edge of a pulse from decoder 4D. 4D is enabled and controlled by the I/O port addresses 48_H thru $4F_H$. Latch 6C maintains the codes on its eight output lines until the next clock pulse from 4D. These codes cannot pass the 8 NAND gates (5C & 7B) until a logic 1 (gate enable) is received from MUX 6E (decoder). The clocking pulse applied to latch 6C is also applied to the CLEAR* pin of 8-bit latch 7C, which clears the latch and sets all 8 "old data" bits to logic 0.

Decoder 4D Action (Figure 3-5)

The Port enabling address at the G1*/G2* pins of 4D is 48_H and ranges up to $4F_H$ when added to the 8 combination codes of the A, B and C1/C2* pins. Decoder 4D applies a falling pulse which clears "old data" latch 7C. When the pulse rises at the end of the I/O cycle, 6C will latch-in the 8 control code signals being held on the data bus by the Z-80.

MULTIPLEXER 6E WITH 8 NAND GATES 5C AND 7B (Fig. 3-6)

Chip 6E (dual 4 line to 1 line MUX, type LS153) provides the function of two separate electronic switches each of which can select from 4 input positions as controlled by a four-combination binary control code applied at pins A and B (fig.3-6).

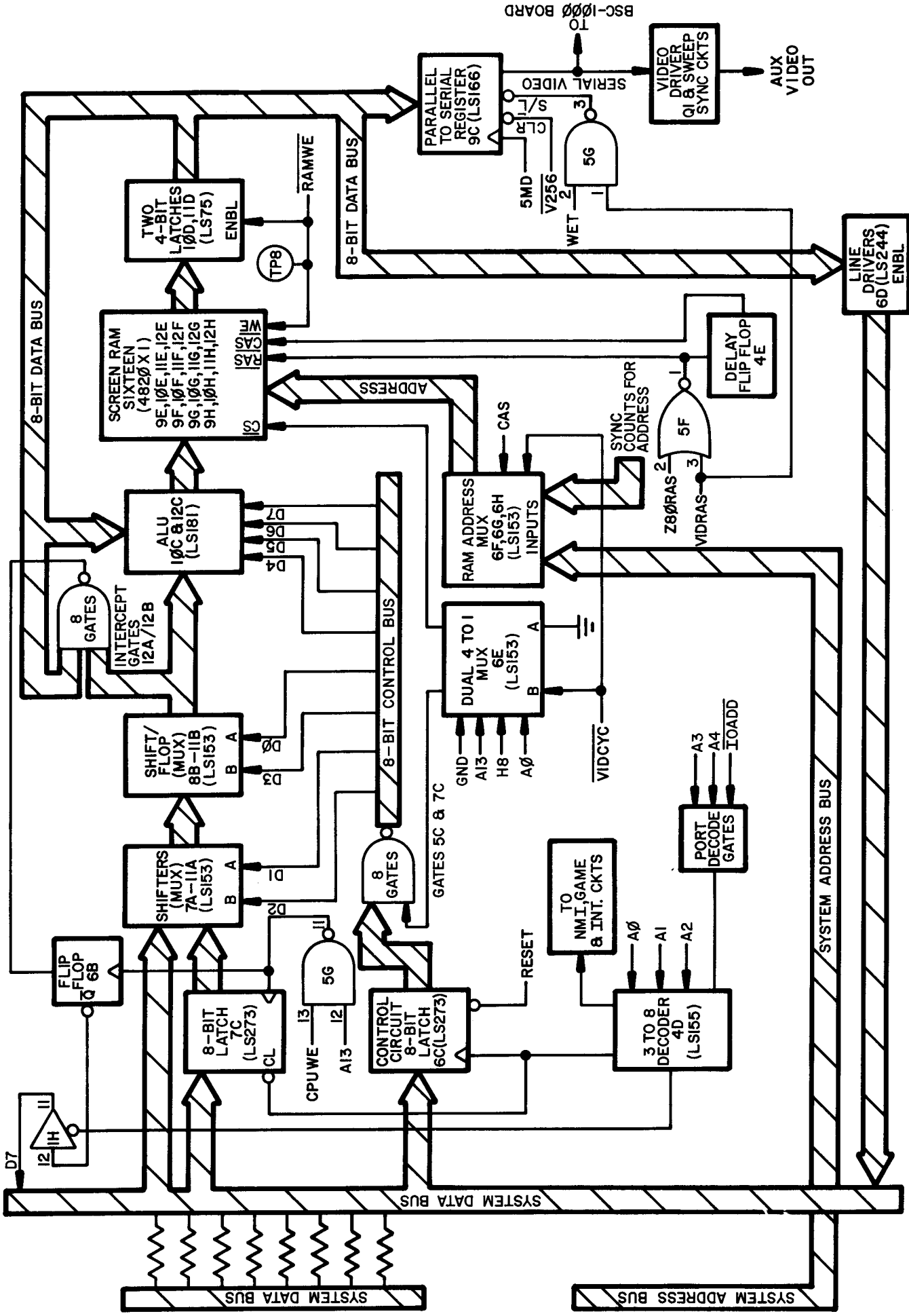


FIGURE 3-5 BLOCK DIAGRAM, VIDEO CIRCUIT GROUP OF VFB-1000 BOARD

However, each of the two switch sections of 6E uses only two of the four possible input positions (ground and A13 for one section: H8 and A0 for the second section. Thus,the chip requires only two binary codes at pins A and B to select the two positions. Pin A is grounded to provide a logic zero at all times and pin B provides the two binary codes of 00 or 10. Pin B is driven by the VIDCYC* waveform derived from an H4 count and the H256 count which are generated in the horizontal counters of the synchronizing system. H4 signal will change logic states every 4 clock pulses (every 800 nanoseconds) and thus will switch the outputs at this rate. The H256 occurs at the end of each horizontal line (after 256 clock pulses) and will disable the decoder during horizontal retrace which lasts for 64 clock cycles, thus adding up to 320 total clock cycles. The following table provides the actions.

Table 3-2. Decoder 6E Actions

CYCLE	B PIN	A PIN	ACTION
VIDCYC*	0	0	A disabling logic 0 is applied to the 8 NAND gates and signal H8 is sent to the RAM for CS*. H8 switches the RAM banks every other video read.
CPU	0	1	Bit A13 is applied to the 8 NAND gates. A13 will enable all gates when it is at logic 1. If A13 is 0, all NAND gates will be disabled causing the video path circuits to pass the data without change.

3.2.1.2 VIDEO PATH CIRCUITS

Shifter/Flopper Circuit Operation

The shifter/flopper circuits consist of nine, dual 4-to-1 multiplexer chips (type LS-153). The chips are: 7A thru 11A and 8B thru 11B (see figure 3-6 chip 6E for the equivalent circuit of the LS153).

Each chip contains the equivalent of two independent electronic switches and thus has two outputs. Each output will be connected (switched) to one of the four associated inputs depending on the binary code applied to the A and B pins (14 and 2 respectively) as follows:

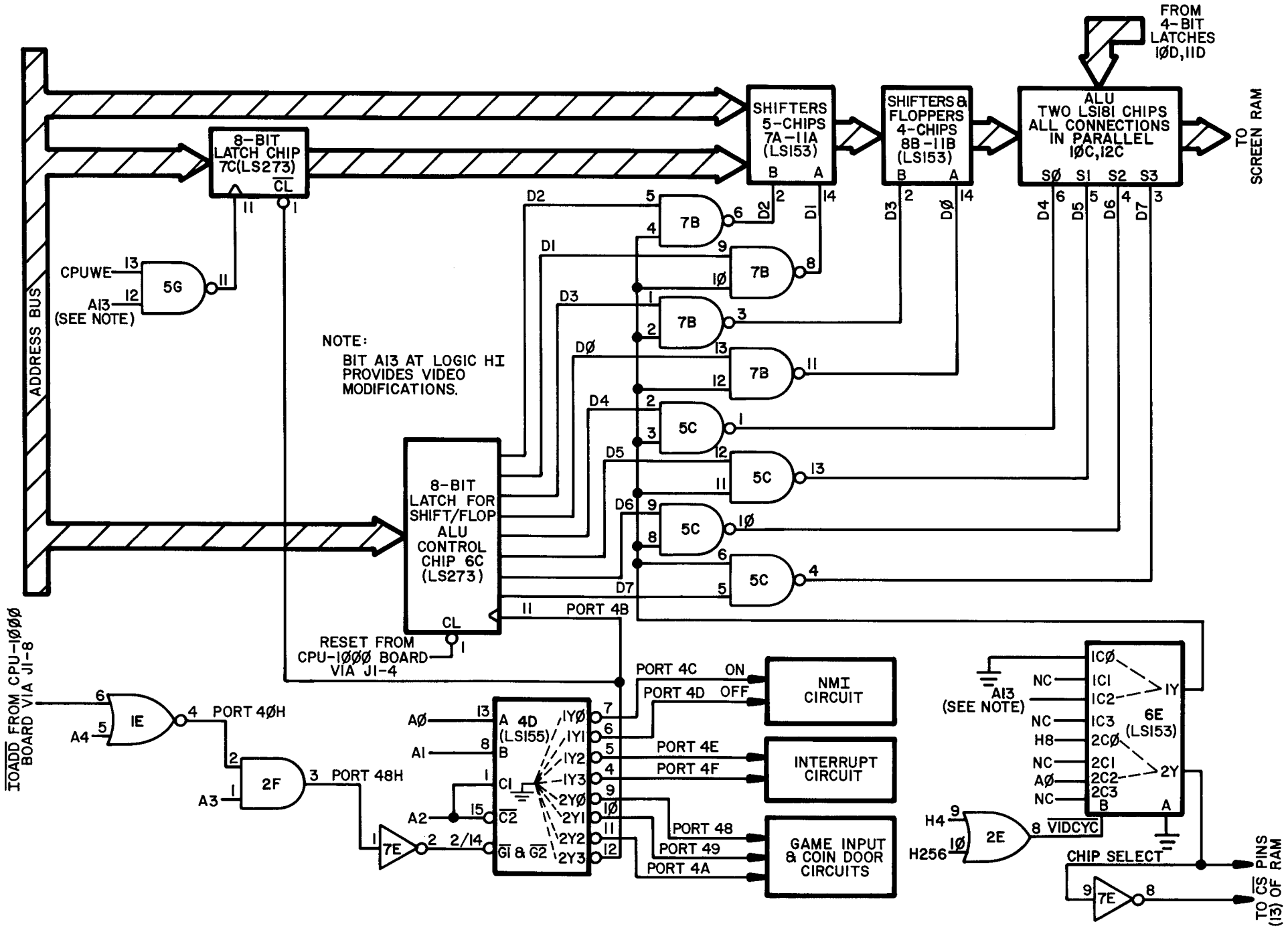


FIGURE 3-6 BLOCK DIAGRAM, SHIFTER/FLOPPER, ALU, MUX 4D & 6D

Input line 3 is connected when B and A are 1 (code 11).

Input line 2 is connected when B is 1 and A is 0 (code 10).

Input line 1 is connected when B is 0 and A is 1 (code 01).

Input line 0 is connected when B and A are 0 (code 00).

The foregoing information applies to both sections. Thus, for code 11, the first section connects to its "3" input (DO on the schematic) and similary the second section connects to its "3" input (D1 on the schematic).

Pins 1 and 15 (strobe 1G* and 2G*, respectively), are provided to enable and disable the two electronic switch sections. In this application both strobe pins are grounded and the chips are permanently active. That is, any signal appearing at the selected input will pass on to the output immediately.

The operation of chips 7A thru 11A can be understood by assuming that a specific binary code is applied to pins A and B and then listing the input signals that will be switched to the outputs as shown in Figure 3-7. For example, if the A and B pins are both logic one (decimal 3) then all the "3" inputs will be picked up and sent to the outputs as follows: D0, D1,D2,D3,D4,D5,D6,D7 and LD0. LD0 means latched data from chip 7C and will be described later. The pattern is orderly and each of the signals will appear on the output lines in an orderly manner. That is, DO will appear on SD0, D1 will appear on SD1, etc. These conditions are illustrated in Figure 3-7 with binary code 11 (decimal 3) shown at the top left. If the binary code is changed to 10 (decimal 2), the conditions are as shown in the second lower group. Code 01 and 00 appear in the third and fourth (lower) groups, respectively.

When binary code 10 (decimal 2) is applied to the 7A-11A chips, the chart indicates that input bits DO and D1 from the System Bus do not arrive at the inputs at all. Also all the data bits from D2 thru D7 have been moved downward so as to replace the missing D0 and D1 bits. The remaining input bit positions are filled by three latched data bits (LDO, LD1 and LD2) received from latch 7C. The total effect, with respect to the CRT presentation, is to move the image byte two bits towards the right side: the reason being that the bytes are applied along each horizontal line with the most significant bit at the left hand side. Thus, if bit 7 is moved to the bit 5 position, the visual effect is a two pixel move towards the right hand side.

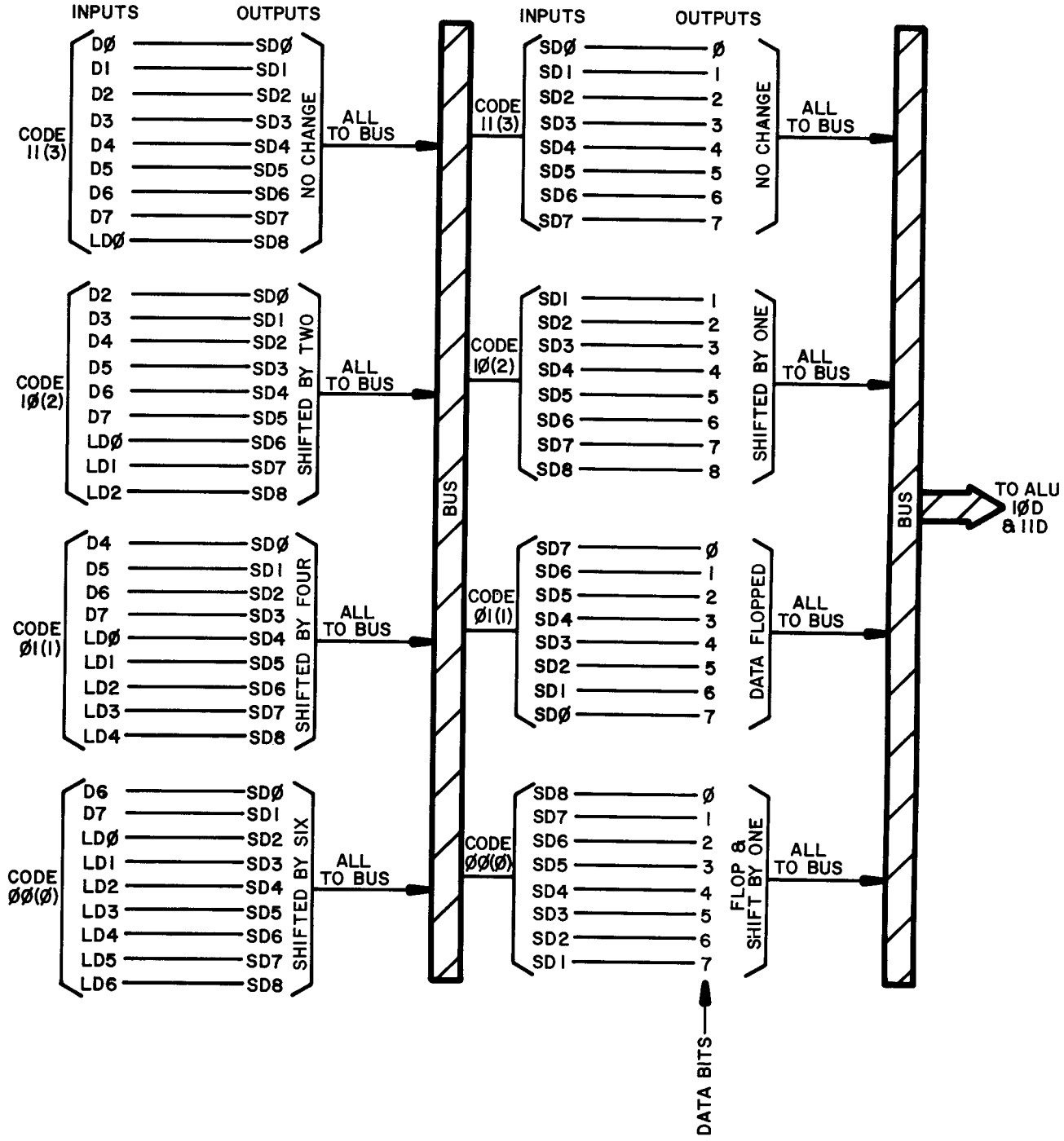


FIGURE 3-7 ACTION DIAGRAM, SHIFTER/FLOPPER CIRCUITS

TOTAL SHIFT AND FLOP FUNCTIONS

The action diagram of Figure 3-7 indicates that a video byte can be unchanged as it passes through chips 7A thru 11A or shifted toward the LSB in steps of 2,4 or 6 (depending on the binary code applied). When passing through chips 8B thru 11B, the video byte can be: (1) unchanged, (2) shifted toward the LSB by 1 bit, (3) flopped so the MSB becomes the LSB and, (4) flopped so the MSB becomes the LSB while simultaneously shifting by one bit toward the MSB.

Combinations of any two of the eight shift/flop paths can be selected by the Z-80 to obtain: steps of 1 thru 7 bit shifts toward the MSB and finally, either of the two foregoing conditions combined with a flop (reversal) of all bits. For example, a shift of three is obtained by passing the byte through the shift-by-two path (code 10 to the 7A-11A chips) and the shift-by-one path (code 10 to the 8B-11B chips). A more complex case would be use of the shift-by-six path (code 00 to the 7A-11A chips) and the flop-and-shift-by-one path (code 00 to the 8B-11B chips). The result is a 7-bit shift toward the MSB with all bits flopped (reversed).

ARITHMETIC LOGIC UNIT

The ALU (Figure 3-6) receives four binary coded signals at pins S0 thru S3 which provide 16 possible combinations. The ALU, which is an LS181 type chip, is capable of performing 16 different logical operations. However, In this application the ALU is working with the video signal which is not only a binary number but also digital video and the quantity of applicable operations is reduced to five.

Two ALU units are used in parallel to provide 8-bit parallel byte handling capability. Each unit has two separate input sections and thus the two ALU units receive two separate 8 bit signals. The "A" input is from the Shifter/Flopper circuit and is a new byte written by the Z-80. The second input "B" is a byte from RAM that has been written at some previous time. The ALU handles the two bytes strictly as two binary numbers but the action can create a modified video signal. The output is the F signal. Typical logical functions performed are as follows:

1. F=A: Input A is transferred to output F unchanged.

2. F=A(XOR)B: Input A is exclusive ORed with input B on a bit by bit basis. This results in electronic erasure of an image when it is compared against itself, and does not affect the surrounding images.

3. F=A(OR)B: Logic value ones of both the A and B signals appear at the F output. This permits an object to be written into an existing background.

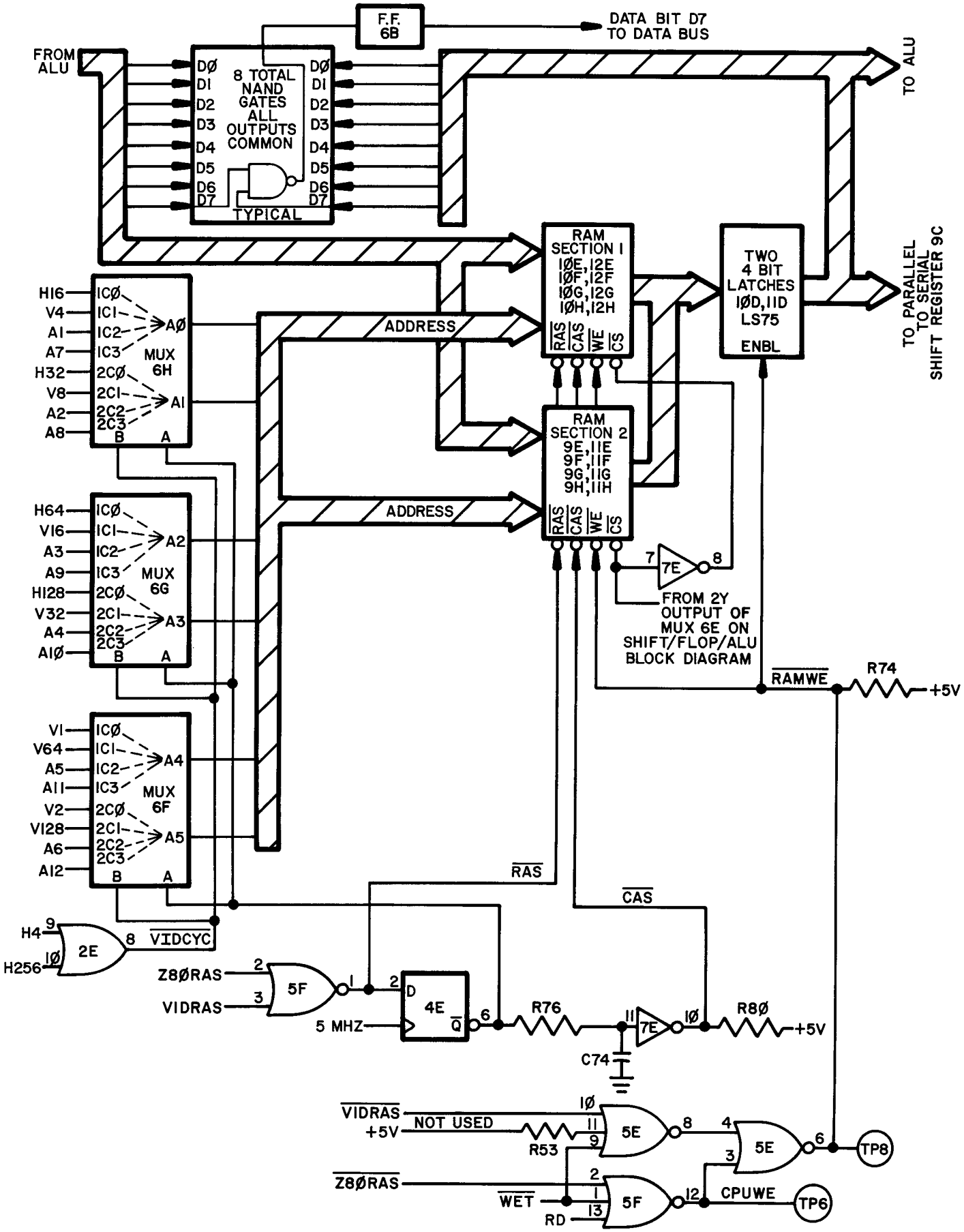


FIGURE 3-8 BLOCK DIAGRAM, MUX 6F,6G,6H AND SCREEN RAM

4. F=A*: Input A appears at the F output in inverted form.

5. F=B*: Input B appears at the F output in inverted form.

RAM Address Multiplexing (Fig. 3-8)

Six address lines (bits A0 thru A5) are applied to the RAM from the three RAM Address MUX chips 6F, 6G and 6H. The three MUX chips receive twelve input signals from two different sources: one of these is the System Address Bus, which is driven by the Z-80 CPU during a "write or read cycle"; the other source is the sync counter circuits which operate continuously and are used during a "video read cycle".

MUX Chips 6F, 6G, 6H Operation

Each of the 3 MUX chips contains the equivalent of two separate 4 pole electronic switches. Thus, there are two outputs on each chip and 4 inputs for each output. See Figure 3-8. Both switch sections on a chip are controlled by the same two binary coded signals applied at the A and B inputs and all 3 chips receive the same code. Thus, for a particular binary code, each of the 3 MUX chips (and all 6 switch sections) will connect one of its 4 inputs to the associated output. The four input poles of each section are designated as: 1C0, 1C1, 1C2, 1C3; and 2C0, 2C1, 2C2, 2C3. The selection code is:

TABLE 3-3. 6-BIT TO 12 BIT MULTIPLEXING

B	A	INPUT SELECTED	TYPE OF CYCLE	SIGNALS
0	0	1C0 and 2C0 (all 3 chips)	VIDEO RAS* CYCLE	H16,H32, H64,H128, V1,V2
0	1	1C1 and 2C1 (all 3 chips)	VIDEO CAS* CYCLE	V4,V8,V16 V32,V64, V128
1	0	1C2 and 2C2 (all 3 chips)	Z-80 RAS* CYCLE	A1,A2,A3 A4,A5,A6
1	1	1C3 and 2C3 (all 3 chips)	Z-80 CAS* CYCLE	A7,A8,A9, A10,A11,A12

12-Bit to 6-Bit Address Multiplexing (Fig. 3-8)

The VID CYC* waveform controls the B pin of MUX 6F, 6G and 6H while the CAS signal controls the A pin. The VID CYC* signal changes state every 4 bits of every byte clocked out to the monitor. Therefore, during each single byte of the video signal, multiplexers 6F, 6G, 6H will perform up to four switching functions. The RAM latches 6-bits of the address at two different time periods as shown by the selection code chart. The first 6-bits of either the video or the Z-80 cycle are latched into RAM by the falling edge of the RAS* waveform while the second 6-bits are latched into RAM by the falling edge of the CAS* waveform. Waveforms are shown in Figures 3-9 and 3-10. The CAS* waveform is a RAS waveform delayed by flip flop 4E, R76, C64 and inverter 7E. The RAM chips contain the necessary internal circuits for latching the two separate addresses and then restoring the full 12-bit code.

RAM INPUT/OUTPUT PATHS (Fig. 3-8)

The RAM is operated in a "Read-Modify-Write" mode whenever a "write" occurs. In this operation, a read occurs first and then a write is activated. Both the read and the write occur during the same cycle of operation and within several nanoseconds of each other. The enabling circuits and waveforms are described later.

During a RAM write, the read phase transfers data to the two 4-bit latches 10D and 11D. The two enable pins of 10D/11D receive the same enabling signal as applied to RAM (RAMWE*) and are activated with a Logic 1 whereas RAM uses logic 0. Thus, 10D and 11D are "transparent" (i.e. with RAMWE* at logic 1, the output follows the "D" input. With RAMWE* at zero, the latches store the last state of the "D" input as related to the time of the logic 1 enable).

Latches 10D/11D hold the data on the 8-bit output bus where it is applied to four circuits: (1) Register 9C, (2) line driver 6B, (3) ALU chips 10C and 12C and, (4) Intercept gates 12A/12B. All circuits are disabled (during write) except the Intercept gates and the ALU.

When a "Z-80-memory-read" occurs, the ALU is set to ignore the read data and line driver chip 6D is enabled to return the data back through the system data bus to the Z-80.

When a "video-cycle-read" occurs, the parallel to serial register 9C is enabled.

Parallel-to-Serial Register 9C (Fig. 3-5)

Register 9C latches the 8-bit video read data at the first clock pulse that coincides with a logic LO Shift/Load* (S/L*) signal at pin 15. When the S/L* pin returns to logic HI, the positive edge of each clock pulse shifts one bit out of the register at 200 nanosecond intervals. Each bit is applied through transistor Q1 for summing with video sync signals to produce a composite video signal. A second output is routed to the BSC-1000 board for color logic.

RAM Read-Modify-Write Function

The read-modify-write action requires the following signal conditions in the time order given.

1st. condition: RAS* changes state from 1 to 0 and latches-in the first 6 bits of the address coming from MUX 6F,6G,6H.

2nd condition: The CS* must change state from 1 to 0 prior to condition 3.

3rd condition: CAS* changes state from 1 to 0 after a delay from the RAS* drop. The second 6 bits of the address from MUX 6F,6G,6H are latched into the chips.

4th condition: WE* changes state from 1 to 0 at which time the write function will occur.

3.2.2 Gating Circuits for VID-RAS Cycle

Figure 3-9 shows the gates and flip flops associated with the waveforms required during VIDRAS operation. Two basic waveforms are generated: VIDCYC* and WET (WRITE ENABLE TIME). The VIDCYC* uses the binary count of H4. This waveform is operable until the end of each horizontal CRT line at which time H256 becomes a logical 1 and disables circuits using VIDCYC* for 12.8 microseconds (horizontal retrace blanking time).

WET uses horizontal counts of H1 and H2* via NOR gate 1E to enable flip flop 1G at the rising edge of each clock pulse. Due to time delays, the FF slips a clock pulse at the leading and trailing edges: The Q output is the WET waveform.

The VIDCYC* and WET waveforms both pass through NOR gate 5F to enable FF 4E at the rising edge of each clock pulse. Time delays again slip a clock pulse at the leading and trailing edges. The Q output is applied to NOR gate 5F to produce RAS*, and via additional circuits, the CAS*. NOR gate 5F also receives the Z-80 RAS waveform when it is generated (See Figure 3-10) and will construct RAS* and CAS* from it. A VIDRAS cycle and a Z-80 RAS cycle waveform never occur simultaneously and no priorty fight exists. However, the horizontal counts of H1, H2, H4 and H256 never stop or change their timing and VIDRAS will always be cycling at NOR gate 5F. This represents the automatic portion of

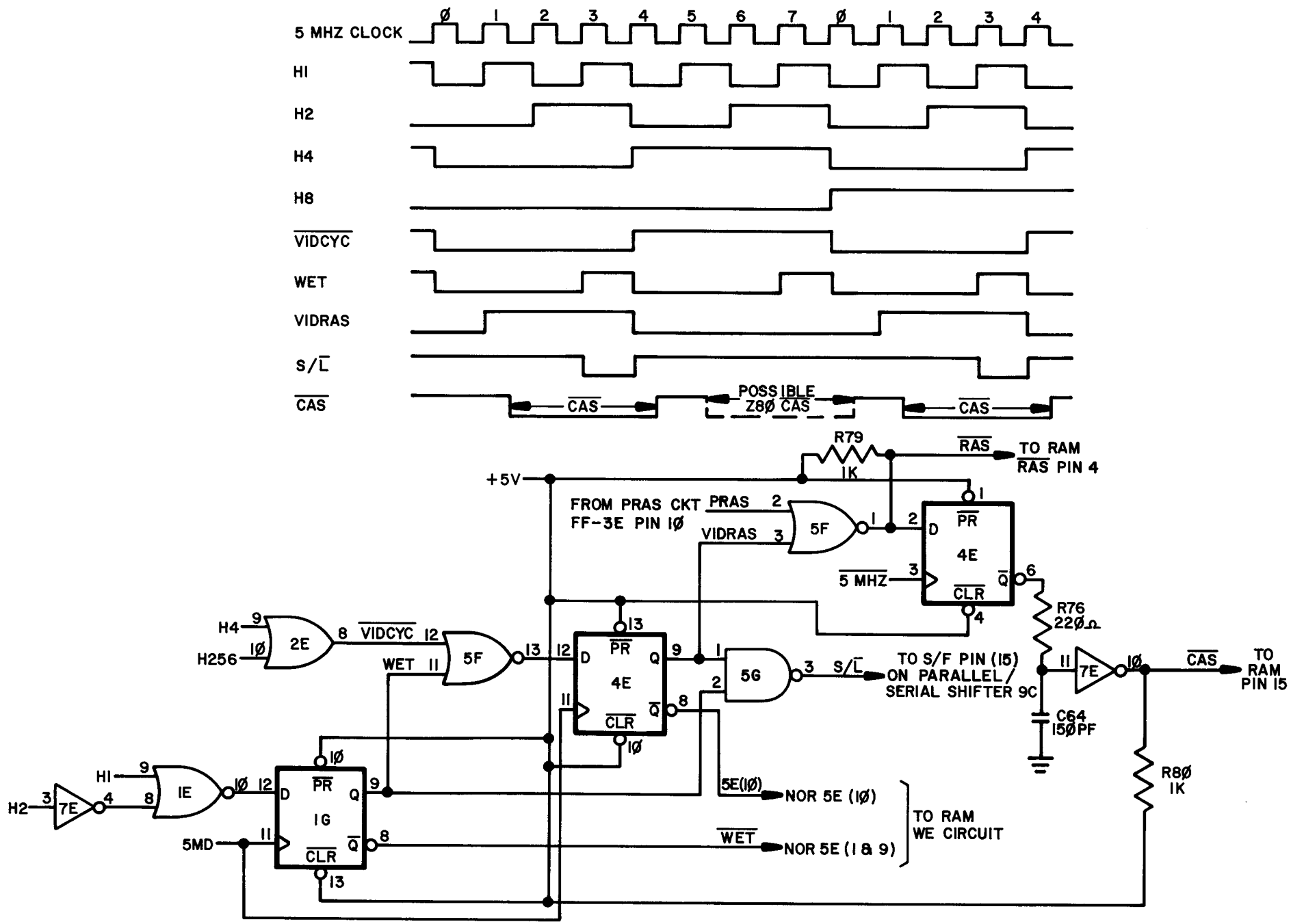


FIGURE 3-9 VIDCYC ,RAS,CAS ,WET, S/L CIRCUITS/WAVEFORMS

the circuit operation as opposed to Z-80 control. The Z-80 controls the Z-80 RAS time and these cycles must essentially be fitted between VIDRAS cycles.

3.2.3 Gating Circuits for Z-80 RAS Cycle

Figure 3-10 shows the gates and single flip flop of the Z-80-RAS waveform generator. The action is clarified by starting at NAND gate 3F which requires 3 logic HI (1) inputs for a logic 0 output. When a 0 output does occur, it will pass thru OR gate 2E with no change when H1 is low, be inverted by NOR gate 5F to a 1 with MREQ* true, and then be applied to the J input of JK flip flop 3E. The PRESET pin of 3E is tied to +5V for a logic HI and allows the CLEAR pin to control the reset action. The CLEAR pin is driven LO after a Z-80 OP-CODE FETCH by the RFSH* line, which CLEARS the FF with Q(Z-80-RAS) at LO (logic 0). The logic 1 from NOR gate 5F will cause the Q output(Z-80-RAS) to go HI after being clocked by the 5M signal. This HI applied to pin 2 of NOR gate 5F (5F is on Figure 3-9) will be inverted to produce RAS*.

Returning to NAND gate 3F (Fig 3-10), the required LO output will occur each time the three inputs of H2, VIDCYC* and Z80 address decode go HI. The HI portion of the VIDCYC* waveform represents a non-active video cycle and insures that NAND gate 3F can provide a LO output only when VID RAS is not occuring.

3.2.4 HORIZONTAL/VERTICAL SYNCHRONIZING SYSTEM

With reference to the schematic diagram for the VFB-1000 board, the two 4-bit binary counter chips 4G and 5H provide a counting cycle of 320 horizontal clock pulses. For the starting point assume that the four output counting lines (H1 thru H8) are set for a logic LO (0) and that a positive clock pulse is applied every 200 nanoseconds (5 MHZ) to all clock inputs.

Counter 4G will count to a total of 15 at which time all outputs are at logic HI (1's) including the terminal count (Tc) line at pin 15. This Tc HI provides an enable to counter 5H at Et (pin 10) so that the 16th clock pulse will be entered into counter 5H to provide a logic HI (1) at output H16 (pin 14). The 16th clock pulse also resets counter 4G to 0000 since 15 is its maximum count. The combination of the two counters 4G and 5H, can normally count up to a maximum of 255 at which time the terminal count (Tc) output (pin 15) of 5H would be used to enable the next counter in the chain, normally at the 256th pulse. However, since the Tc output is coupled back to the LOAD input at pin 9 (via inverter 3H) and is also applied to the J input of flip flop 2G, the 256th clock pulse will load counter 5H with the binary code applied at the A,B,C and D inputs and a count will not be entered into counter 3G. Inputs A and B are grounded (logic 0) and will always load 00. Inputs C and D are tied to the Q* output of flip flop 2G and will load the Q* state. Since the 256th pulse sets Q HI, C and D will both be HI (1) and the total count into counter 5H will be binary 1100, or a decimal count of 192. Binary 1100 at counter 5H is actally equal to binary 11000000 since pin C

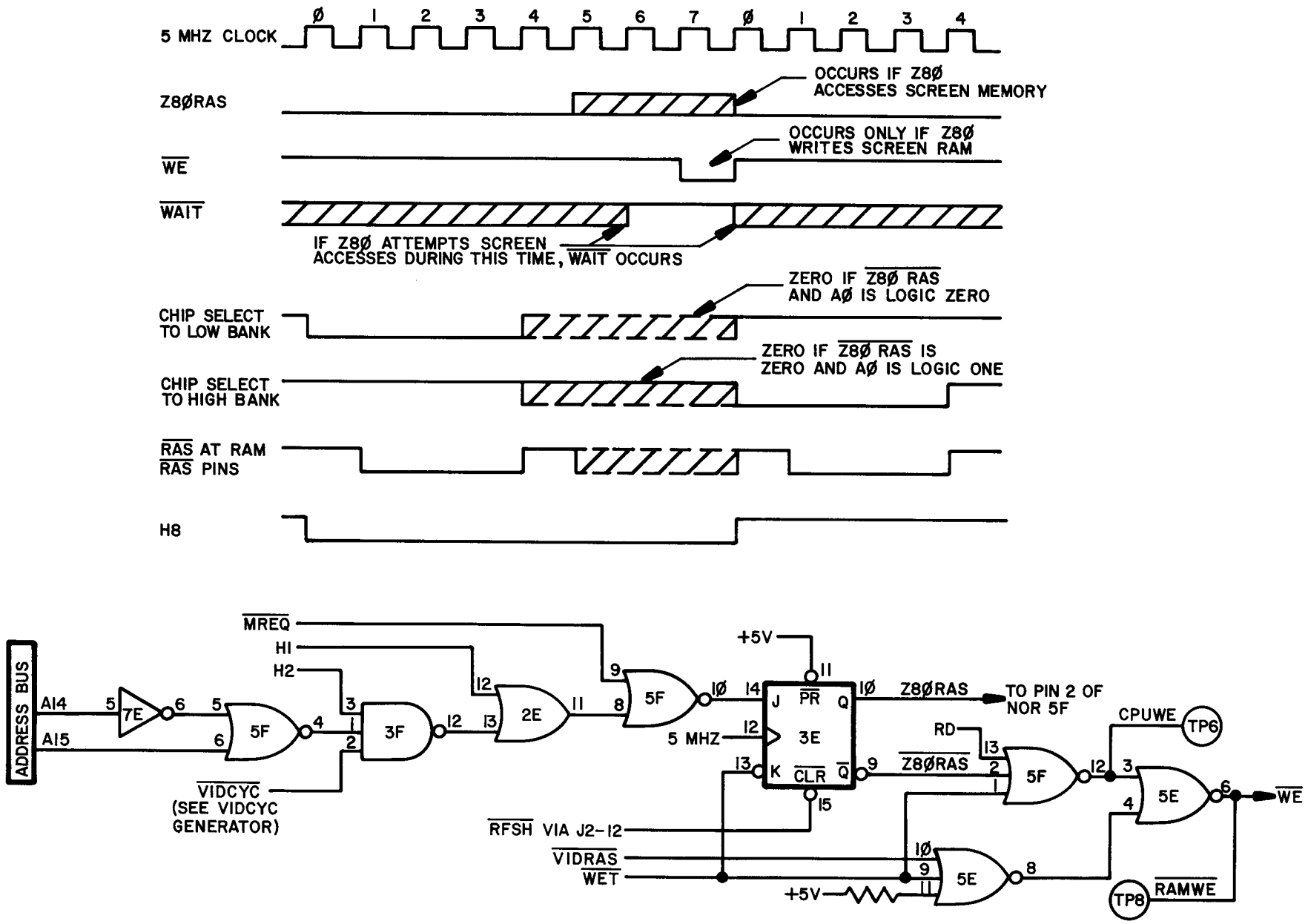


FIGURE 3-1Ø RAS AND WE CIRCUITS WITH WAVEFORMS

equals 64 and pin D equals 128.

With a decimal count of 192 loaded into counter 5H, 64 more clock pulses will be required to raise the count to 255 (maximum count of 5H). At count 255, the Tc output will again go HI.

Before continuing, it is necessary to realize that the 255th pulse is actually pulse number 319, because the two counters had already reached a count of 256 before counter 5H was loaded with decimal 92. Thus, the true total count in 5H is 256 counts-plus-63, or 319.

At count 320, the Tc output of counter 5H will apply an enable pulse to vertical counter 3G. Each time horizontal counter 5H reaches a count of 320, counter 3G will be incremented. Thus, 320 horizontal counts equal 1 vertical count. There will be 262 vertical count pulses for each video frame on the CRT.

The gating circuit comprised of inverter 3H and NAND gate 3F generates the HSYNC* pulse to the monitor.

Vertical counters 3G and 4H are connected to start a counting cycle when V32 is logic HI, or more accurately, with 4H at an output count of 2 in hexidecimal. This occurs because flip flop 2G has its Q output (V256) at a logical 1 as a result of the previous counting cycle. Shortly after the initial load occurs, the flip flop will toggle, bringing V256 false. This point is the start of displayed video and is a RAM address of 400_H.

The counter chain will be advanced one state per horizontal line until 223 lines of video are displayed. At this time, counter 4H output at the Tc pin will go to logic 1, which loads count 218 (decimal) into the counters via inverter 3H (pins 8&9). Flip flop 2G now toggles, bringing V256 to logic 1, and starting the vertical blanking interval. The gate circuit comprised of NOR gate 1E and NAND gate 3F combine V256, V16, V8 and V4 to generate VSYNC*, which is combined with HSYNC* in AND gate 2F to generate CSYNC* (composite sync). After 38 additional horizontal lines, flip flop 2G again toggles, restarting the timing sequence, and beginning a new frame of video. Thus, 262 horizontal lines comprise one frame of video of which 223 lines are used for picture and 39 occur during blanking and sync.

3.2.5 INTERRUPT CIRCUITS (FIGURE 3-11)

Interrupts are used to inform the processor of the vertical position of the CRT electron beam with respect to either the middle of the screen or the end (bottom) of the screen. This data is used by the Z-80 to confine screen RAM pattern changes to the non-displayed half of the screen. Pattern changes made in the active portion of the screen could result in disturbing visual patterns. The system is programmed so the software always changes images in the half of the screen that is not being used (displayed). The interrupt circuitry generates the middle screen and end screen interrupt signals.

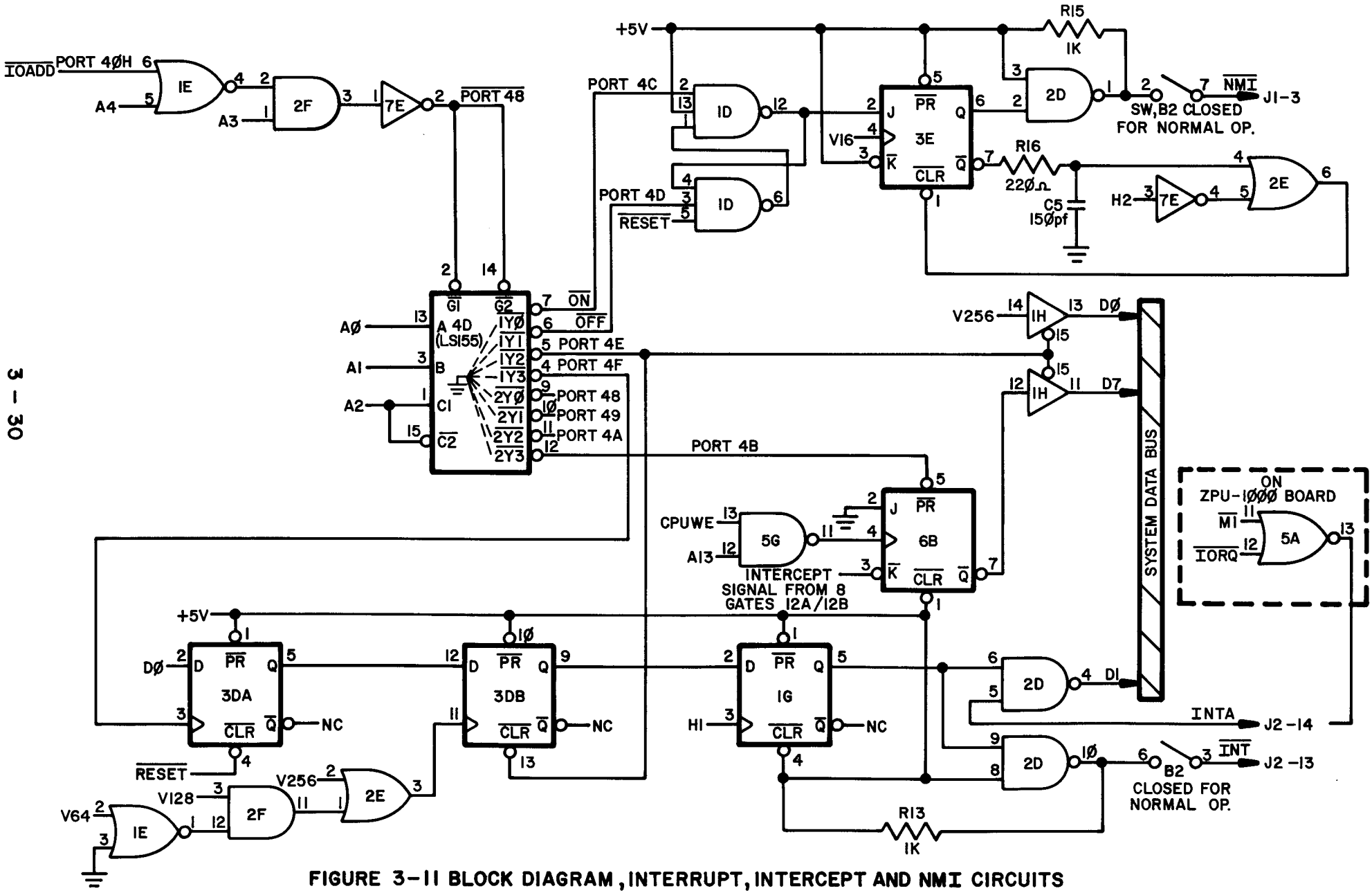


FIGURE 3-11 BLOCK DIAGRAM, INTERRUPT, INTERCEPT AND NMI CIRCUITS

The interrupt circuit is enabled by the Z-80 writing a logic 1 to port $4F_H$. This results in the Q (pin 5) of latch 3Da being set to logic 1. Note that the RESET* signal disables the interrupts by clearing latch 3Da. Gating comprised of NOR gate 2E, NAND gate 2F, and NOR gate 1E generates a positive going edge at the middle and end of screen....specifically, when V128 changes state. This signal is used to clock latch 3Db, transferring a logic one to its Q output. Latch 1G is used to synchronize interrupt signals with the Z-80 clock, which is essentially the same signal as H1. When the Q of 1G goes HI, open-collector inverter 2D (pins 8,9 & 10) asserts the INT* line which is applied back to the Z-80. Switch B2 is used to break the interrupt feedback path during Signature Analysis testing.

If the internal interrupt circuits of the Z-80 are enabled, it will respond by bringing its M1* and IORQ* lines true simultaneously. This causes NOR gate 5A (pin 13) on the ZPU-1000 board to go HI, asserting INTA (interrupt acknowledge). Gate 8G (pins 3 & 4) on the ZPU board applies a zero to data bit D0 at this time. NAND gate 2D (pins 4,5,6) on the VFB board applies a zero to data bit D1. Data bus lines D2 thru D7 are pulled high by resistors on the ZPU board. Thus, vector FC (hex) is fed back to the Z-80 causing it to jump to its interrupt handling routine. A register inside the Z-80 (the "I" register) points to the top 8 bits of the interrupt handling address, and is software programable. The returned Vector is applied to the lower 8-bits of the address bus. The Z-80 reads this and the following address. This "read" data then forms another address to which the processor is directed. This address is the beginning of the interrupt acknowledge routine, and will vary from game to game.

Part of the interrupt routine will be to read from port $4E_H$ which causes the following three conditions.

1. The interrupt is cleared by clearing latch 3D. This removes the zero from the INT* line.

2. V256 is applied to bit D0. This will signify a mid or end screen interrupt (zero for the mid screen and 1 for the end of screen).

3. The Q* output of latch 6B is applied to bit D7. This will signal that an intercept has occured in a previous screen RAM write (zero for no intercept or, 1 for intercept).

3.2.6 NON-MASKABLE INTERRUPT CIRCUIT (FIGURE 3-11)

The NMI* is used as a general timer, and occurs at a 480 Hz rate (2.08 millisec). Typically this is used to update sounds. The NMI* circuit is made maskable so it can be disabled by the software. The NMI* will be disabled whenever sounds are not being generated. Either a RESET*, or a write to port 4D, will disable the NMI circuitry. A write to port 4C will enable the circuit. Flip flop 1D makes up the enable latch. Flip flop 3E is the NMI*

generator and it is enabled when its J pin (2) receives a logic 1. The FF is clocked by vertical sync signal V16. The rising edge of V16 will bring the Q output (pin 6) of 3E to logic 1. This level is inverted by open collector inverter 2D (pins 1,2,3), and asserts the NMI* line to the processor. The processor will now jump to location 0066 and execute the NMI routine stored there. The jump to 0066 is an inherent hardware feature of the Z-80.

The Q* output of the flip flop 3E is delayed by R16 and C5 and then applied to OR gate 2E, along with an inverted version of horizontal address counter output H2, from inverter 7E. This circuit serves to clear the NMI* signal after two system clocks have occured. The total circuit is comprised of latch 3E, R16, and C5. OR gate 2E and inverter 7E form a one-shot multivibrator that is clocked by V16, and enabled by latch 1D. Switch B2 is used to break this feedback path during Signature Analysis.

3.3 BUFFER SYSTEM COLOR BOARD (BSC-1000)

The BSC-1000 board generates an R-G-B type of color signal from the black/white digital video generated by the VFB-1000 Board.

The color board electrically divides the entire screen into 4 X 4 (pixel) "color boxes" which can be considered as an overlay to the digital video.

Any pixel within a color box can be set to any one of sixteen colors as commanded by the software. Black pixels within the 4 X 4 box will not be changed and will be displayed as black.

Any white pixel within the box will be displayed with the color value previously stored for that box.

The color displayed for any non-zero (white) pixel within a color box is set by four bits as follows:

```
      RED.....1=on    0=off
    GREEN...1=on    0=off
     BLUE....1=on    0=off
INTENSITY....1= full on   0=1/2 intensity
```

Thus, 16 colors (two of which are black) can be displayed for any white (non-zero) pixel within the box, while black is displayed for any black (zero) pixel.

Horizontal and vertical address bits, from the counters on the VFB board, read-out the color overlay RAM in sequential order. The low RAM bank (processor addresses 8000-83FF) is read out during the top half of the screen (V128 equals zero) while the high bank (Processor addresses 8400-8FFF) is read out during the bottom half of the screen (V128 equals 1).

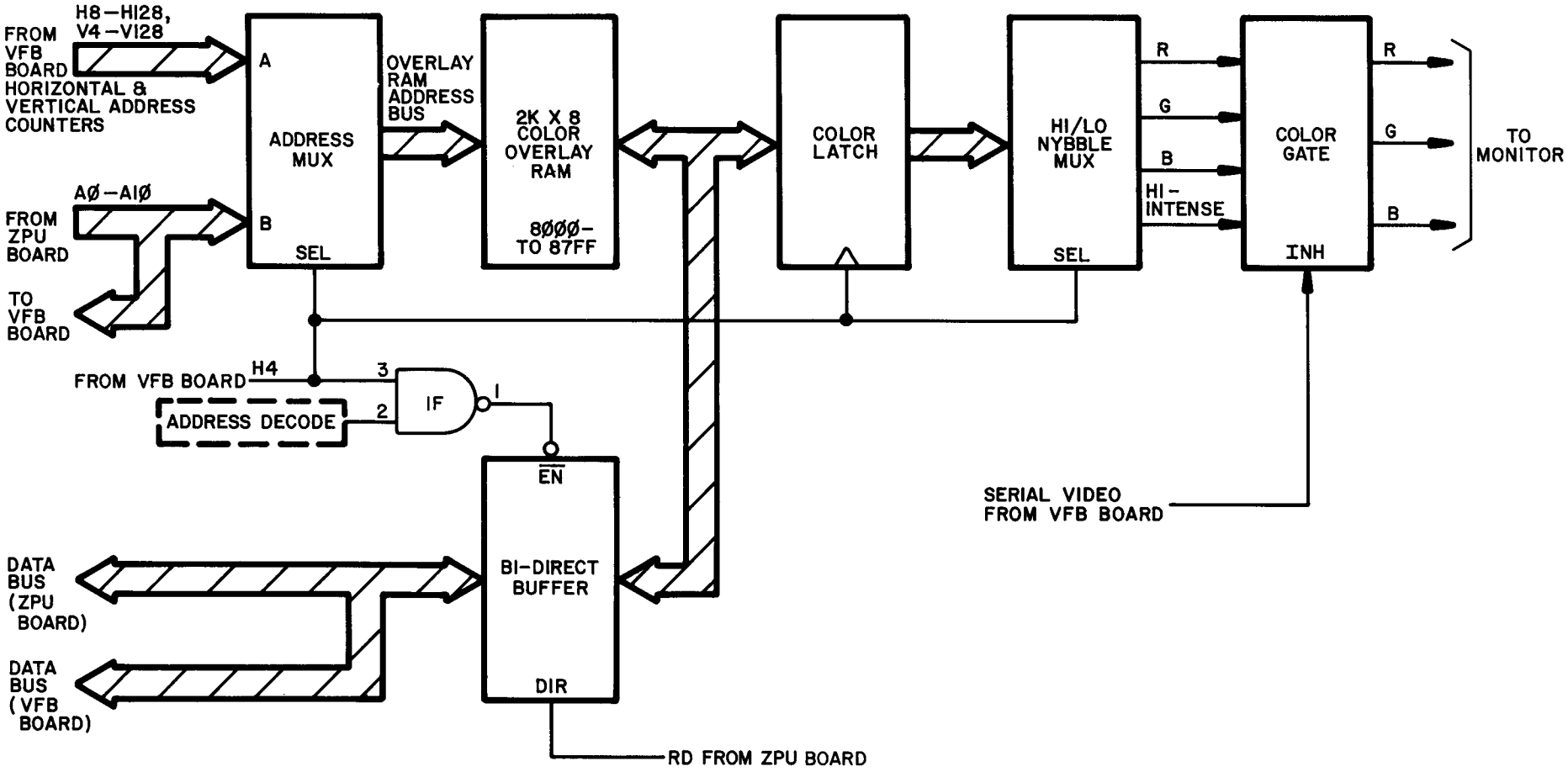


FIGURE 3-12 BLOCK DIAGRAM, BUFFER SYSTEM COLOR BOARD (BSC-IØØØ)

A full byte is read out at any specific cycle, but only 4 bits (one nybble) of the byte are used at a time. A latch stores all 8 bits and a quad two-input multiplexer is used to sequentially apply the color nybbles to the color gating circuits.

The color gating circuits combine the 3 color bits, the intensity bit and the serial video to produce R, G and B outputs to the monitor. Three switches are provided to adjust the low intensity color drive to compensate for variations in the TV monitor input circuits. Address decode and control circuits are provided to read and write data from-and-to the RAM. To permit the processor to read/write RAM data, and to generate WAIT* states (if a RAM access is attempted while the color values are being accessed), RAM address multiplexers are provided.

The foregoing information indicates that the color coder overlay RAM functions by defining 4 control bits to signify the color to be displayed for a non-zero pixel (in any 4 x 4 pixel box on the screen).

During the time H4 is zero, the video address counter bits H8 thru H128, and V4 thru V128 are used to address color RAMS 2A and 1B thru 3B via Quad 2-to-1 muxers 4A, 4B and 4C. Each nybble that is read will define the colors to be displayed in that box.

The muxers address an 8 bit word, which is Latched, and then used 4-bits at a time. The rising edge of H4 is used to latch the color overlay data into latch 2C. When H4 is logic 1, the CPU address bits A0 thru A10 are used to form the RAM address space.

Control gate NAND 1F (pin 1) will go to logic 0 during a color overlay RAM access if H4 is at a logic 1...indicating that a video "read" is not in progress. This zero-going signal enables bus buffer 3A, connecting the processor data bus to the color overlay RAM data bus. Data direction thru the buffer depends on the RD line: logic 1 gives a read-out of the RAM while a logic 0 writes data into the RAM.

Inverter 1D, (pins 8 and 9) and NAND gate 1F (pins 4, 5 and 6) combine video addresses H4 and H2 such that pin 4 is logic 0 when H4 is logic 1, and H2 is logic 0. This signal defines the time during which a RAM write can occur. D flip flop 2E shifts video address H1 by 90-degrees in phase and this signal is used to clock the other section of FF 2E. The D input to this stage is the above mentioned "write time slot", and will permit a RAM write to occur if the logic zero is removed from PRESET pin 10 by NOR gate 1E (pin 8). NOR gate 1E (pin 8) will be at logic 1 when the Z80 accesses address 8000_H-$87FF_H$. With these conditions, flip flop 2E (pin 9) will go to a logic zero 90-degrees (or 100 nanoseconds) after H4 goes to a logic 1, and H2 goes to a a logic 0. NOR gate 1E (pin 12) will go to logic 1 if RD is at logic 0, implying a write is occuring. This signal is input to NOR 1E (pin 3), and also inverted by gate 1D, which forms the write signal to all 4 RAMS.

NOR gate 1E (pins 3, 4, 5, 6) combines the "write-to-address space" signal with what is essentially a "READ-from-address-space" signal to generate a zero going edge which activates the chip select signals to the RAMS. This gating insures that the address bus has settled before the chip select signal becomes active (a timing requirement of the 2114 RAM). The described zero going edge is combined with H4 in NAND gate 1C (pins 11, 12 & 13). Keep in mind that H4 is at 0 during a color overlay "READ". To sum up the conditions, NAND gate 1C (pin 11) will go to logic 1 under the following conditions:

1. A read or write relative to addresses 8000_H-$87FF_H$ (if H4 is 1).

2. When H4 is 0, a color overlay read is implied.

NAND gate 1C (pins 1 & 2) generates the chip select for the low order RAM bank (2A, 1B). NAND gate 1C (pins 4, 5, 6) generates the high order RAM (2B, 3B) chip select. Input signals to pins 2 and 4 are generated by the above mentioned signals (1C, pin 11) while the state of address multiplexer 4A (pin 9) determines the logic level at the other inputs. During Z-80 access time, the RAM chip select is determined by the state of address line A10, while during "overlay-READ-time", the chip select is determined by video address V128. Thus, the low order RAM is displayed during the top half of the screen....and the high order during the bottom half.

If the Z-80 tries to access RAM at any time other than when H4 is zero and H2 is a one, NAND gate 1F (pin 13) will put the Z-80 into WAIT* until the conditions are correct.

Switch F2-1 is used during Signature Analysis Testing to open the WAIT* line to the CPU.

NAND gate 2D (pins 8, 9,10) generates MEMRD*, a signal used for signature analysis.

Color overlay data is read while H4 is a logic 0. Each 8-bit "read" is latched into octal latch 2C, by the rising edge of H4. H4 also forms the select input to multiplexer 3C. This multiplexer connects each color overlay control nybble to the color gating circuits at the proper time. The high order nybble bits 4-7, are displayed first (H4 is logic 1) while the low order nybble is displayed last (H4 is logic 0).

Either bit 0 or bit 4 is defined as RED. A logic 1 in either bit implies that the red gun in the CRT is turned ON. Either bit 1 or 5 is green with the same definition as red. Either bit 2 or 6 is blue and is defined the same as for red. Either bit 3 or 7 is the intensity control: when the bit is logic 1, the associated color guns are "full on". A logic 0 gives one-half of full intensity.

NAND gates 2D and 3D combine the RED, GREEN, BLUE and INTENSITY signals with the serial video-bit-stream generated by the VFB-1000 board to provide control signals to the digital-to-analog converters formed by "open-collector" inverter 3E (plus a resistor and switch network). All three colors are generated in the same manner so only the operation of the RED circuit will be described.

If the color bit is a logic 1 and the serial-video bit stream is a logic 1, then the output of NAND gate 2D will go to logic 0. This disables inverter 3E, removing the ground from the junction of R13, R16 and R19. Assuming that the intensity bit is logic 0, then the output of NAND 3D is logic 1 and the output of inverter 3E (output pin 12) is logic 0. Therefore, a ground is applied to resistor R13 by inverter 3E. Thus, a voltage divider is formed resulting in a RED output voltage of +3.75 volts if switch F2-2 is open, and +2.47 volts if the switch is closed. This switch is used to compensate for the variations in half levels between the Wells-Gardner and the Electrohome monitors. The switch is closed for Electrohome and open for Wells-Gardner.

If the intensity bit is a logic 1, the output of NAND gate 2D is still a logic 0, and inverter 2 (pin 2) is logic 1 (OFF). However, the output of NAND gate 3D is now at a logic 0 which turns OFF the output (pin 12) of inverter 3E. The ground is now removed from R13 and the RED output line rises to +5V. Resistor R16 provides this pull-up function. The green and blue gate circuits operate in a similar manner.

3.4 VOICE SYNTHESIZER UNIT (BOARD VSU-1000)

The voice generator chip is essentially a special purpose microprocessor used to generate sounds recognizable as human speech. It does this by electronically simulating the human vocal tract through a programmable 10 stage digital lattice filter. Filter coefficients are stored as binary patterns in the voice PROMs and are loaded into the filter under the control of the processor. Input signals for the filter originate in either a tone generator or a noise generator. The generator selection is also under the control of this processor. The decision as to which generator is to be used is determined by the word sound to be generated. The pitch or tone of the resultant word is controlled by the frequency of the input clock which is, in turn, determined by the programmable clock divider as controlled by the Z-80.

A word is generated when the Z-80 writes a word-number to the voice generator command port (44_H or 54_H) depending on strap option W3 or W4, respectively...and the status of D7 and D0 of the Data Bus. The Z-80 will have previously set-up the pitch and volume. The one-to-zero transition of the word latch clock waveform will trigger one-shot 2B, while the zero-to-one transition will latch the word number into "word latch" 5B. The resultant stretched positive pulse will command the voice

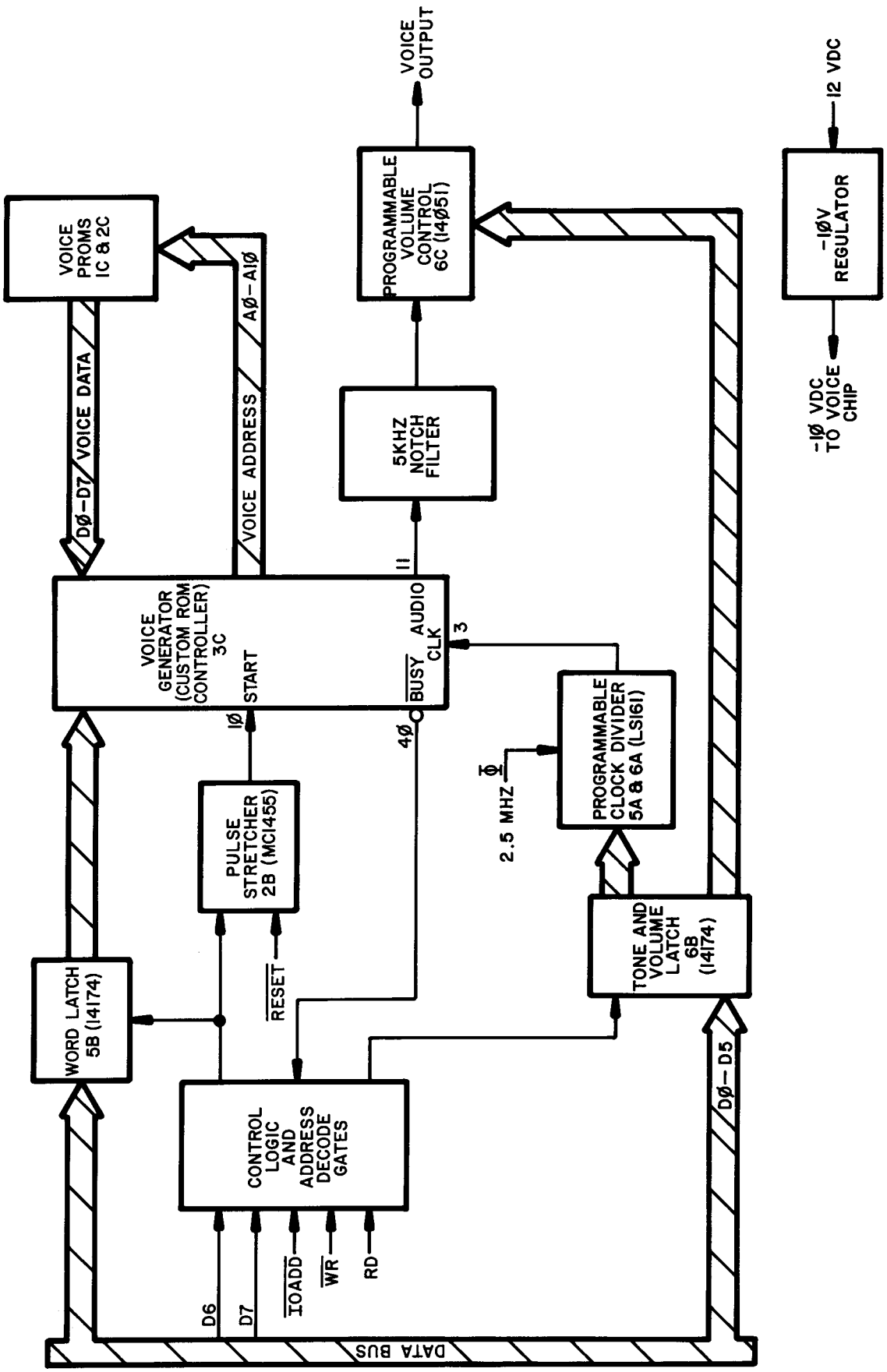


FIGURE 3-13 BLOCK DIAGRAM ,VOICE SYNTHESIZER UNIT (VSU-1000)

generator 3C to begin saying the selected word. The word will actually begin at the falling edge of the "start" waveform. The period of the pulse stretcher one-shot is about 2 usecs, a set-up time required by the voice generator.

The voice generator then addresses the PROM to obtain the filter parameters for the lattice filter, and sets the BUSY* output to logic HI (indicating that the chip is busy). The chip will continue to get new parameters until it has finished saying the selected word. It should be noted that the Z-80 only communicates word numbers, and that the word associated with a given number will vary from game to game. The data to make an actual word is stored in voice PROM 2C and possibly 1C (depending on the game).

When the selected word has been completed, the voice processor asserts (brings LO) the BUSY* bit, indicating it is NOT BUSY. While the system is saying a phrase, the Z-80 will occassionally (usually every 2 milliseconds) monitor the status of the BUSY* bit. Whenever the voice generator is NOT BUSY, the Z-80 can request the next word number in the phrase.

3.5 SOUND BOARD (SB-1000) CIRCUIT OPERATION

The prime component of the sound board (SB-1000) is the 6840 programmable timer module. It contains three, 16-bit, programmable timers and several control registers. The 6840 has the capability of generating interrupts based on values input (applied) to the counters....but this feature is not used. Input clocks for these counters can come from two places, the chip's ENABLE input (pin 17) which is a sub-multiple of the system clock, or instead, the separate clock which arrives at the C* input. There are separate C* input pins for each counter but in this system all three pins are connected together. An internal register selects which source will supply the clock signal to the programmable counters...or tone generators. If the enable pin (17) is selected, 2.5 MHz clock/4 (625 KHz) signal clocks the generator. Otherwise, the output of a random noise generator clocks the generators. This is useful for producing noise-modulated tones, such as accelerating engine noises.

Decoding circuits comprised of decoder 6A, XOR gate 8A, AND gate 9B and two gates in inverter 7B select ports 40 through 47 when jumper W1 is connected. The same circuits will select ports 50 through 57 when jumper W2 is connected. Both jumpers must not be connected at the same time.

AND gate 10B (pins 1, 2, and 3) buffers the system clock. A shift register made up of a dual D flip flop (chip 10C) divides the clock by four resulting in a 625KHz clock. This divided and phase-shifted clock generates other SB-1000 bus interface timing. Specifically, this waveform clocks D flip flop 9C, at pin 3.

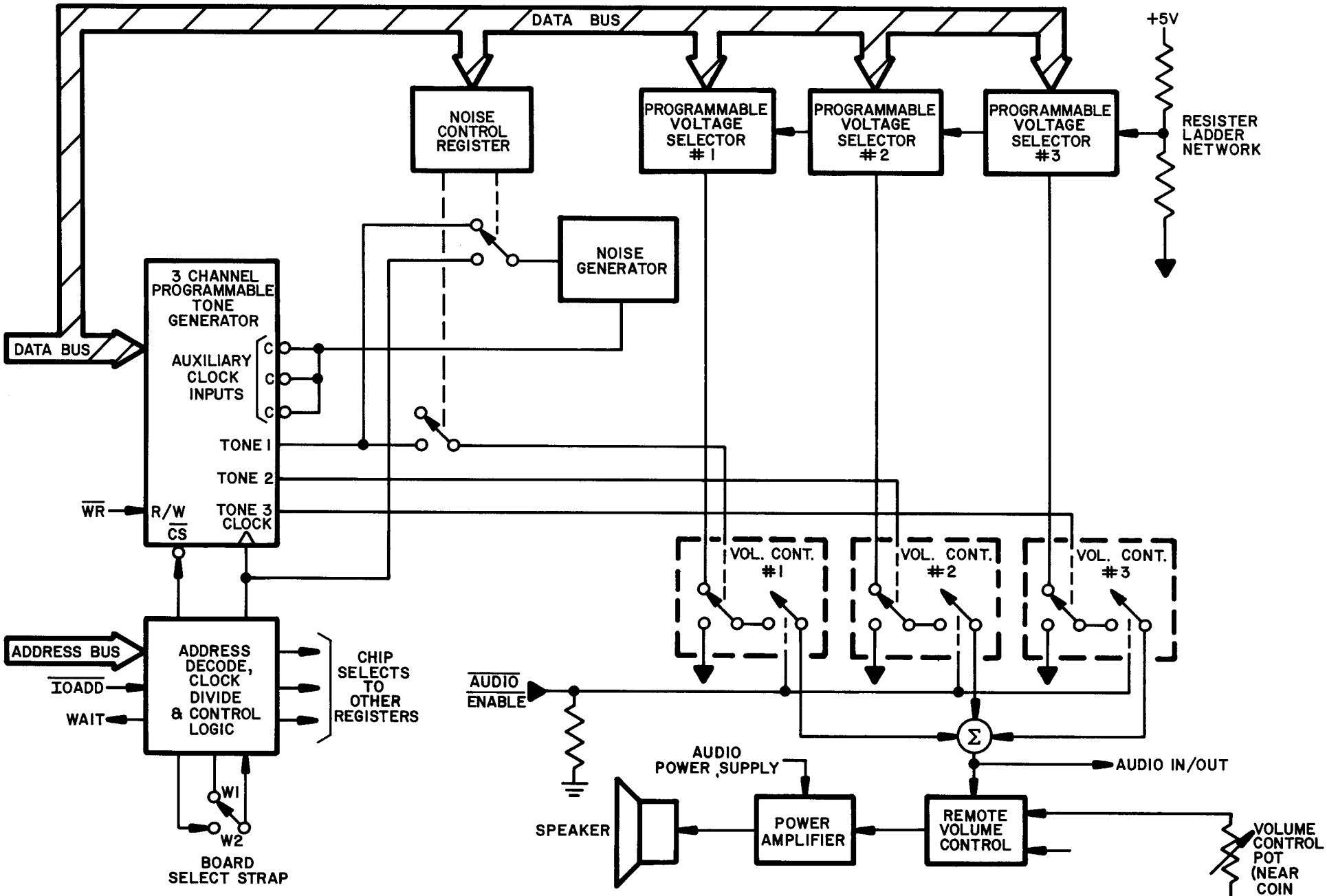


FIGURE 3-14 BLOCK DIAGRAM, SOUND BOARD (SB-1000)

Whenever port addresses 40 through 43, 45 and 47 are accessed, AND gate 9B (pin 11) goes to a logic HI, removing the CLEAR from flip flop 9C, pin 1.

Since flip flop 9C, pin 13 was being held clear (because 9C, pin 1 was clear) then its Q* pin (8) is logic HI. Therefore, since 9B pin 11 has gone HI upon receipt of the port decode described, NAND gate 9A, pin 4 goes to a logic LO, asserting the WAIT* line. This does not affect the Z-80 at this time since it is in a T2 cycle.

The next processor cycle is a self-induced WAIT* state. During the falling edge of the 2.5 MHz signal, the status of the WAIT* line is sampled. Since the SB-1000 board previously pulled WAIT* LO, a wait state will occur at the next processor "T" state. One or two of these WAIT* states will be inserted, depending on the state of the "E", or enable line of the 6840. After either one or two more 2.5 MHz rising edges, (clock) pin 3 of flip flop 9C will go to logic 1 causing CSO* of the 6840 to go LO and activating registers within the 6840. At the same time, the clear (pin 1) will go HI, storing data into the 6840 or gating it onto the bus, and also bringing the D-input (pin 12) of flip flop 9C HI. The next 2.5 MHz falling edge, inverted by 8A, will cause 9C pin 8 (Q*) to go LO, removing the WAIT* signal from the Z-80. The Z-80 will now go into a T3 state, which results in the 6840 access ending due to the following: the address decode waveform goes LO, clearing both sections of flip flop 9C, ending the cycle, and preparing the circuitry for the next 6840 access.

WAIT* states are only generated by the board during a 6840 access. Dip switch 10B breaks the WAIT* connection back to the Z-80 for signature analysis testing. The switch should be closed for normal operation.

As mentioned earlier, one of the clock sources for the tone generators is the system clock divide circuit (D type flip flop 10C). The other source is a psuedo-random noise generator. Shift register 7A (type 4562) is the prime component of the noise generator and has 128 D-type flip-flops in it. Output Q96 and Q128 are exclusive-ORed together to form a random pattern of logical ones and zeros. This output is fed to a two stage shift register made of Dual D flip-flop 8B. The clock to the first stage is the same as that to shift register 7A, while the second stage of 8B receives the inverted clock. Thus, the second stage shifts the phase of the random bit pattern by 90 degrees, satisfying the setup time requirements of the 4562 shift register, 7A.

Since shifter 8B is only one stage in length, exclusive OR gate 8A (pins 8,9 and 10) feeds back a signal displaced in time by one clock pulse. This insures randomness in the pattern, (i.e. noise). The 8B flip flop PRESET (pin 10) also serves to "seed" the noise generator. Without this configuration, an illegal condition will occur if, upon power up, all stages (including 8B) of the shift register come up with zeros. A logic one loaded into

this stage by the RESET* signal prevents this condition from occuring.

Output Q96 of shift register 7A is fed to the C1*,C2* and C3* pins of the 6840 where it can be selected as a clock source to the tone generators.

Multiplexer 6B (pins 1,2,10 and 15) selects the clock source to the noise generator. When pin 10 is a logic one (Port 46_H Bits 7 and 6 at zero, and Bit 0 at 1) the noise generator clock will be 625 KHz (2.5 MHz/4). MUX 6B (pin 10) taken to a zero will select tone 1 as the clock source. Thus, a prescale of the noise clock can be used to develop various noise frequencies. Gate 6B (pins 3,4,5 and 9) is used to develop the drive required for inverter 7B (pins 10 and 11). Multiplexer 6B (pins 11,12,13 and 14) prevents the tone from reaching the amplifier when it is used as the noise clock.

Registers 2A, 3A & 4A, along with Analog Multiplexers 2B, 3B & 4B form a software programmable voltage selector. Voltages generated by a resistor ladder network made up of R2, R1, R19, R18, R16, R17, R15 and R14 are channeled to the X pin of each analog multiplexer under the control of the register. This voltage then forms the logic 1 voltage to each of three volume controls. Each volume control is basically a two-to-one multiplexer. One input to the multiplexer is the above mentioned "one" level, the other input is analog ground. The control signal is the tone output of the 6840. When the output is at a one, the "one" level previously selected appears at the output. When the tone generator output is a zero, analog ground appears at the output. Thus, the overall volume of a tone, plus the envelope can be controlled by software. In addition an audio output enable is provided by R10. If pin 1 of connector J3 is taken to a logical one, all SB1000 generated audio can be turned off. The outputs of all three volume controls are summed together in a network comprised of C2,C3,C4 and R6, R7, R8 and R11. The result can be summed with an external audio signal input injected into J3 pin 3. The voice audio generated on the VSU-1000 is injected at this point. The resulting audio is fed to the "remote control attenuator" (3C). An external pot (mounted inside the coin door) and connected between pins 6 and 8 of connector J3 will function as the master volume control. A low-pass filter made up of R21, R22, C25 and C27 applies the audio signal to power Amplifier 8C, and stablizing feed back is provided by R24,R27 and C24. The amplified audio is sent to the cabinet speaker at connector J3, pins 9 and 11.

The VATEN supply (J3 pin 7) is a +12 volt regulated supply for the volume control chip. Pin 12, VAUD10 is a +15 volt max power supply for the audio amplifier. All other power for the SB1000 comes from the +5 volt regulated supply.

3.3.6 PHOTO REFLECTIVE UNIT (PRU-1000)

The PRU-1000 (Photo Reflective Unit) consists of four opto

reflector modules and a comparator. Each opto-reflector module is comprised of an infa-red LED which is emitting continuously and emits infra-red light upward to a reflective conical washer. A photo-darlington transistor, which is sensitive to infra-red light, is mounted alongside the LED in the same enclosure.

When the game's joystick control is moved, it causes the conical washer to be moved into the beam of one or more of the LED's. The resultant angle of the conical washer is such that the emitted infra-red light is reflected into the photo-darlington, causing it to turn ON. The geometry of the system is designed such that at maximum deflection from the center, the conical washer is no closer than 0.125 inch from the surface of the photo reflector. The output of each photo darlington transistor is applied to the positive, or non-inverting, input of an LM339 comparator. All the negative (Inverting) inputs are connected together to a biasing network composed of R2, R3 and C1 which trips the comparator at +3.75 VDC. Capacitor C1 is used to decouple any noise.

The output of each channel of the comparator is normally high since the photo darlington transistors are usually OFF. When a transistor turns ON due to movement of the joystick, the voltage on the positive input of the comparator will go below that of the negative input (used for the reference level) causing the comparator output to go to a logical 0. This logical-0 is input to the switch buffers on the VFB-1000 board and is interpreted by the software to be an instruction to move (or fire) in the direction indicated by the joystick position. Diagonal movement or firing is accomplished by activating two adjacent sensors.

3.7 POWER SUPPLY (PS-1000)

3.7.1 Operation on 120 or 240 VAC

The power transformer has a split primary winding which must be connected in parallel for a 120 VAC line or connected in series for 240 VAC operation. A 6.3 Vac secondary (10 & 11) provides power for general illumination on the coin door. A 120 Vac secondary (12 & 13) is used as an isolation winding for powering the monitor.

3.7.2. Positive 5 Volt Supply

An 8 Vac winding is used as the logic power supply and is protected by F3, a 5 amp. fuse. A full wave bridge rectifier (diodes CR1 through CR4) rectifies this voltage and capacitor C1 filters it. This voltage is +5 unregulated and is available at pin 1 of J3 and J4. This voltage is also connected to the +5 volt regulator which is mounted on a separate heat sink. A 5 volt adjustment pot (R2) is provided to insure that the supply voltage is proper at the load. The +5 volts regulated supply is available at jacks J3, J4 (pins 2,3 and 4). The supply should be adjusted to provide between +5 and +5.25 Volts as measured at test point 4

(TP4) on the VSU-1000 board.

3.7.3 Positive 12 Volt Supply

A center - tapped secondary of the transformer (terminals 7, 8 and 9) supply the other voltages required for the game. The center tap is grounded. Diodes CR5 & CR6 make up a positive full-wave rectifier. Fuse F1, a 3A Slo-Blo, protects the positive supply. Capacitor C2 filters the +12 unregulated supply, which is available at jacks J3 & J4 (pins 14). This supply is connected to two regulators, VR1 & VR2, which are mounted on a heat sink. VR1 is a +12 volt regulator, with output available at jacks J3 & J4 (pins 6 & 7) and a voltage test point for measurement at TP4. The voltage measured should be between +11.4 and +12.6 volts Vdc. VR2 is a +15 volt regulator which receives its power from a +12 Vdc unregulated supply. Its output is measured at TP3. This regulator is used to limit the maximum voltage available to the Power Amplifier to protect it. The regulator output is generally +8 Vdc to +14 Vdc.

3.7.4 Negative 12 Volt and 5 Volt Supplies

Diodes CR7 and CR8 form a negative, full wave rectifier, protected by fuse F2, a 3/4 Amp Slo Blo type, and filtered by C3. This -12 volt unregulated power is available at J3 & J4 (pin 15). Voltage regulator VR3, a -5 volt regulator is fed by this supply and its output is available at jacks J3 & J4 (pins 5 and 8). This voltage can be measured at TP2, and should be between -4.75 and -5.25 Vdc. All four of the voltage regulators contain over current shut-down circuits.

Care should be exercised when working in the area of the power transformer since line voltage is available at terminals 1,2,3,4,12 and 13 of the transformer. It should also be noted that lethal voltages are available at several places on the color monitor.

SECTION 4
TROUBLE SHOOTING BY SELF-TESTS

4.1 PERTINENT INFORMATION

1. The following tests occur each time the RESET button is momentarily pressed or when power is removed and re-applied.

2. The self-test indicating LED is on the ZPU-1000 board (CR45) and each indicating flash is accompanied by a tone from the sound system.

3. The LED stops flashing at the malfunction provided all PC boards are connected in the system.

> NOTE:
> If the ZPU-1000 board is not connected to the VFB-1000/BSC-1000 board combination, the self test program will continuously cycle and counting LED flashes is meaningless. Also, if the SB-1000 board is not connected, or if it is defective, no self-test tone will be generated.

FIRST SELF TEST

The first of 8 LED flashes occur accompanied by a tone from the speakers. This first test analyzes the ROM circuits on the ZPU board.

ANALYSIS OF FIRST TEST WHEN LED STAYS ON

Continuous illumination of the LED indicates problems in one or more of the following areas:

1. The POWER-ON RESET circuit. Check NAND gate 7G, inverter 8G and associated circuits.

2. Loss of clock signal. Check oscillator transistor Q12. flip flop divider 8A and other associated components.

3. Microprocessor (Z-80) is defective (Chip 7B).

4. Defective Address Bus (shorted or open) or control buffers (chips 6B and 7D, type LS244).

5. Defective PROM chip(s).

6. Defective I/O Decode Circuit. check chips 5A, 4A, 6A, 7G and decoder 7E.

7. Defective LED latch. Check chips 7G, 3A, and 8G.

Analysis of First Test when LED Flashes Once and stays OFF. This symptom indicates the problem is in one or more of the following areas.

1. Defective PROM circuitry. Check all PROM chips since the malfunction may be in any one chip.

2. Defective Address Decode Circuit. Check chips 6E, 4A, 5A, 6A and 8G.

SECOND SELF-TEST

The second of 8 LED flashes should occur accompanied by a tone from the speaker. This test analyzes the "scratch pad" area of the RAM on the ZPU-1000 board. For the following diagnostics, the LED must flash twice and extinguish.

ANALYSIS OF SECOND TEST

NOTE: All following chips are on the ZPU-1000 Board.

1. Check RAM CHIPS 1E and 2E.

2. Check transistor Q2 and associated components/circuits.

3. Defect in gating chips 2A, 3A and 6A.

4. Check that the jumper used for chip 1E (W5, W6 or W11) is correct for the particular chip part number. Refer to paragraph 3.1.2 for details.

THIRD SELF-TEST

The third of 8 LED flashes should occur accompanied by a tone from the speaker. This test analyzes the RAM (screen RAM) located on the VFB-1000 board. For the following diagnostics, the LED must flash three times and extinguish.

NOTE: The following chips are on the VFB-1000 Board.

1. The CRT will display a RAM chip location map which will indicate a defective chip. Mentally rotate the map 90 degrees counter clockwise to properly orient the map with the lower right hand portion of the VFB-1000 board. If the defect is not located, use the following steps:

2. Check the +12V and -5V voltages, specifically to the VFB-1000 board.

3. Check RAM address Multiplexers 6F,6G,6H and 6E.

4. Check the RAS* and CAS* circuits: chips 4E, 7E, 1G, 5G and 5F.

5. Check the "RAM write" circuits: chips 5F and 5E.

6. Check the Address/Arbitration circuits, chips 5G, 5F, 7E, 3F, 1F and 2D. Check that switch 2B (contacts 4 & 5) is set to the ON position.

7. Check the "magic" enable circuits of chips 7B and 5C.

8. Check the "write" data path of chips 7A, 8A, 10A, 11A, 12C and 10C.

9. Check the "Read" data path of chips 10D, 11D and 6D.

10. Check all Bus connectors, especially J1 and J2 on both the VFB-1000 and BSC-1000 boards.

FOURTH SELF-TEST

The fourth flash plus a tone tests the RAM circuits on the BSC-1000 color board. 1F the LED stops on the fourth flash, perform the following listed tests:

NOTE: All following chips will be on the BSC-1000 board.

1. Check RAM chips 3B, 2B, 1B, and 2A.

2. Check the Address Multiplexer chips 4C, 4B and 4A.

3. Check that DIP Switch 2F (pins 4 & 8) is set to the ON position.

FIFTH SELF-TEST

The fifth flash plus tone tests the Shifter/Flopper circuits on the VFB-1000 board. If the LED stops on the fifth flash, perform the following tests.

1. Check Shifter/Flopper chips 7A, 8A, 9A, 10A, 11A, 8B, 9B, 10B, 11B.

2. Check ENABLE gates 7B and 5C.

3. Check control latch 6C.

4. Check "OLD DATA" latch 7C.

5. Check Port Decoder 4D.

SIXTH SELF-TEST

The sixth flash plus a tone tests the Arithmetic and Logic Unit (ALU) and the intercept circuits on the VFB-1000 board.

NOTE: All following listed chips are on the VFB-1000 board.

1. Check ALU chips 12C, 10C.
2. Check ENABLE gate 5C.
3. Check the Intercept gates 12A, 12B.
4. Check Flip-Flop 6B and associated gates of 5G and 1H.

SEVENTH SELF-TEST

The seventh flash plus a tone tests the Interrupt and Non Maskable Interrupt (NMI) circuit portions which are on both the ZPU-1000 and VFB-1000 boards. When the LED stops at the seventh flash, perform the following tests:

1. Check that Dip Switch 2B (pins 3-6 and 2-7) is set to on.
2. Z-80 microprocessor.
3. Interrupt generating circuitry 1G, 3D, 2D.
4. Time Gating circuity 1E, 2F, and 2E.
5. NMI ENABLE Latch 1D
6. NMI generating circuitry 2E, 3E & 2D.

EIGHTH SELF-TEST

If the LED indicator and associated tone have occured eight times, the malfunction is either in a circuit that is not within the testing capabilities of this self-test program or the problem is unique such as an intermittent condition that changes with physical movements or temperature.

After eight flashes have been obtained, try the game to see if the problem has been removed by the check-out action. If the game operates properly, it is advisable to attempt to locate the former problem by checking all connectors for tightness. Also lightly tap various areas while viewing the CRT.

If eight flashes have occured and the game is still inoperable, the following information outlines the circuits that are not part of the self-test routine and must be verified by other test methods:

1. Check the settings of all DIP switches on the ZPU-1000 and VFB-1000 boards by setting switch S9 (on ZPU-1000) to ON and then pressing the RESET* button (on ZPU-1000). The CRT will display the ON/OFF conditions of all switches which must then be checked against the Installation and Operating manual data.

2. Visual analysis of the CRT pattern (when it is available) can provide many clues to circuit operation as described in the following paragraphs. Total loss of the CRT display usually indicates problems in the monitor itself.

3. Malfunctions in the horizontal or vertical address counting circuitry, or SYNC generator circuits will cause "bad" video to be displayed. Vertical or horizontal stripes should give an indication of where the error is. A rolling or flipping picture is an indication of SYNC problems, either in the monitor or on the VFB-1000 board SYNC circuits.

4. Color splotches are an indication of a malfunction in the color gating circuitry, or a monitor problem. Check BSC-1000 board chips 2C, 1C, 2D, 3D, 3E and associated switches and resistors.

SOUND SYSTEM PROBLEMS

1. NO SOUND; Check amplifier 8C on the SB-1000 board. Check VAUDIO (+15V MAX).

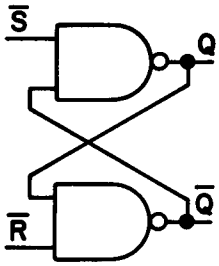
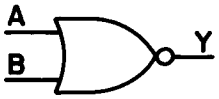
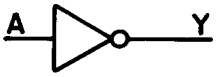
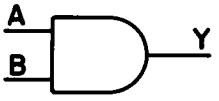
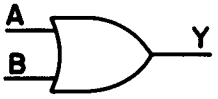
2. Voice is normal but there are no sound effects: Check the 6840 chip on the VSU-1000 board. On this board check that Dip Switch 10B (pin 1-8) is in the ON condition. Check the addressing and timing circuitry chips 6A, 8A, 9B, 9A, 9C, 10C, 8A and 10B. Any other malfunction will result in either the loss of a specific sound or, a change in a sound and can thus be identified as a related circuit.

3. Sound effects are normal but there is no voice: Check VSU-1000 chips: CRC ROM chip 3C, PROMs 1C,2C, clock generator 5A, 6A, decode & control logic 1A, 2A, 3A, 4A, 2B, 5B, 6B, 6C. Also check the -10V supply (on the board). Distorted Noise: check PROM 1C, 2C, CRC ROM chip 3C, filter & amplifier 5C.

APPENDIX A TRUTH TABLES FOR LOGIC UNITS

NOTE: WHEN REFERRING TO THE TRUTH TABLES, USE THE FOLLOWING DEFINITIONS.

1	LOGICAL ONE, GREATER THAN +2.4 VOLTS
0	LOGICAL ZERO, LESS THAN +0.8 VOLTS
X	DON'T CARE, EITHER ONE OR ZERO
HI-Z	OFF, NEITHER A ONE OR A ZERO
↑	A ZERO TO ONE TRANSISTION
↓	A ONE TO ZERO TRANSISTION
QN^*	THE STATE OF THE OUTPUT AT THE LAST ACTIVE TRANSISTION OF THE CLOCK OR CLEAR.

FUNCTION	SYMBOL	TRUTH TABLE
$\overline{S}$ $\overline{R}$ FLIP FLOP TYPE LS00		
NOR TYPE LS02		
NOT TYPE LS04 7406		
AND TYPE LS08		
OR TYPE LS32		

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	QN	$\overline{QN}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

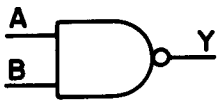
A	Y
0	1
1	0

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

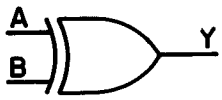
FUNCTION | **SYMBOL** | **TRUTH TABLE**

NAND
TYPE LS00
7401



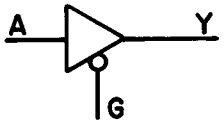
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

EXCLUSIVE OR
TYPE LS86



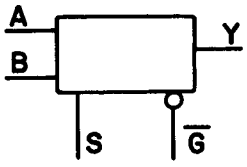
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

TRI-STATE BUFFER
TYPE LS244
LS367



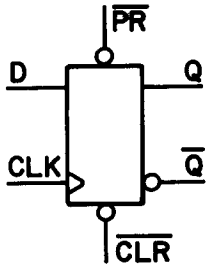
A	G	Y
0	0	0
1	0	1
0	1	HI-Z
1	1	HI-Z

TWO-INPUT MULTIPLEXER
TYPE LS257



A	B	S	$\overline{G}$	Y
X	X	X	1	HI-Z
0	X	0	0	0
1	X	0	0	1
X	0	1	0	0
X	1	1	0	1

D-TYPE FLIP FLOP
POSITIVE EDGE
TRIGGERED WITH
PRESET AND CLEAR
TYPE LS74



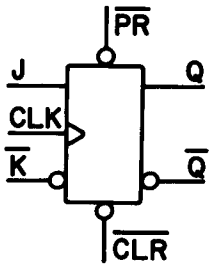
$\overline{PR}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	QN	$\overline{QN}$

* DENOTES UNSTABLE CONDITION

FUNCTION | **SYMBOL** | **TRUTH TABLE**

J-K FLIP FLOP WITH PRESET & CLEAR

TYPE LS109

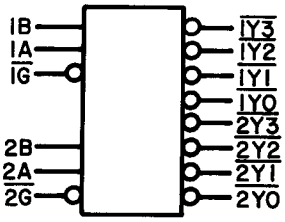


$\overline{PR}$	$\overline{CLR}$	CLK	J	$\overline{K}$	Q	$\overline{Q}$
0	1	X	X	X	1	0
1	0	X	X	X	0	1
0	0	X	X	X	1*	1*
1	1	↑	0	0	0	1
1	1	↑	1	0	T	T
1	1	↑	0	1	QN	$\overline{QN}$
1	1	↑	1	1	1	0
1	1	0	X	X	QN	$\overline{QN}$

* DENOTES UNSTABLE CONDITION
T DENOTES TOGGLE

DUAL 2-LINE TO 4-LINE DECODER

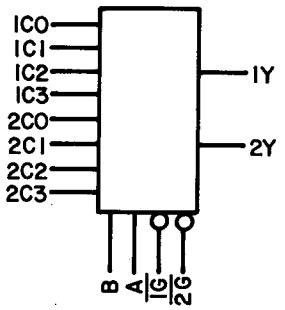
TYPE LS139



$\overline{G}$	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

DUAL 4-LINE TO 1-LINE DATA SELECTOR

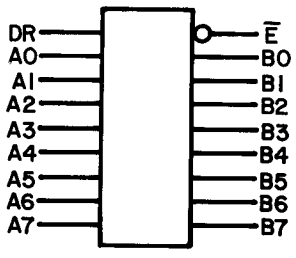
TYPE LS153



B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

OCTAL BUS TRANSCEIVER

TYPE LS245



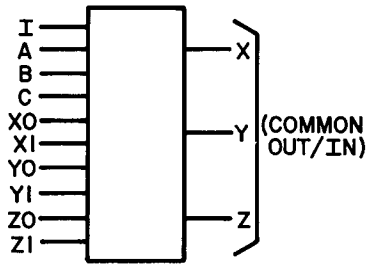
$\overline{E}$	DR	A & B
0	0	B TO A
0	1	A TO B
1	X	HI-Z

FUNCTION

8-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER

TYPE 4053

SYMBOL



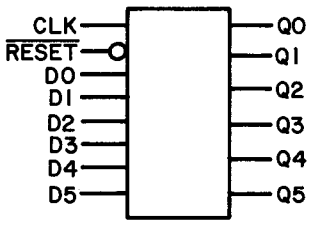
TRUTH TABLE

I	A	B	C	SWITCHES
1	X	X	X	OFF
0	0	X	X	XO TO X
0	1	X	X	XI TO X
0	X	0	X	YO TO Y
0	X	1	X	YI TO Y
0	X	X	0	ZO TO Z
0	X	X	1	ZI TO Z

I DENOTES INHIBIT

CMOS D-TYPE FLIP FLOP

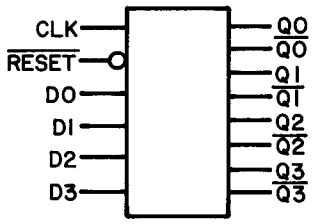
TYPE 4174



$\overline{\text{RESET}}$	D	CLK	Q
1	0	↑	0
1	1	↑	1
1	X	↓	QN
0	X	X	0

CMOS D-TYPE FLIP FLOP

TYPE 4175



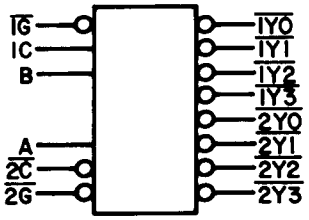
$\overline{\text{RESET}}$	D	CLK	Q	$\overline{\text{Q}}$
1	0	↑	0	1
1	1	↑	1	0
1	X	↓	QN	$\overline{\text{QN}}$
0	X	X	0	1

FUNCTION

DECODER

TYPE LS155

SYMBOL



TRUTH TABLE

B	A	$\overline{G}$	1C	$\overline{2C}$	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
X	X	1	X	X	1	1	1	1
0	0	0	1	0	0	1	1	1
0	1	0	1	0	1	0	1	1
1	0	0	1	0	1	1	0	1
1	1	0	1	0	1	1	1	0
X	X	X	0	1	1	1	1	1

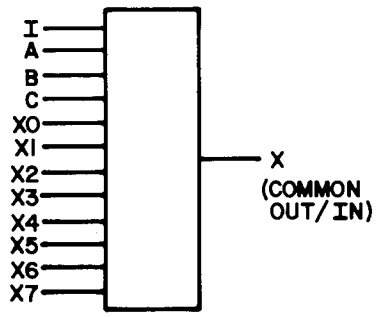
IF CONNECTED AS DUAL 2-LINE TO 4-LINE DECODER

1C	$\overline{2C}$	B	A	$\overline{G}$	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y2}$	$\overline{2Y3}$	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	X	X	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	0	1	0	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1
0	0	1	1	0	1	1	1	0	1	1	1	1
1	1	0	0	0	1	1	1	1	0	1	1	1
1	1	0	1	0	1	1	1	1	1	0	1	1
1	1	0	0	1	1	1	1	1	1	1	0	1
1	1	1	1	0	1	1	1	1	1	1	1	0

IF CONNECTED AS A 3-LINE TO 8-LINE DECODER

8-CHANNEL ANALOG MULTIPLEXER/ DEMULTIPLEXER

TYPE 4051



I	C	B	A	SWITCHES
0	0	0	0	X0
0	0	0	1	X1
0	0	1	0	X2
0	0	1	1	X3
0	1	0	0	X4
0	1	0	1	X5
0	1	1	0	X6
0	1	1	1	X7
1	X	X	X	OFF

I DENOTES INHIBIT

PARTS LIST FOR
VIDEO FRAME BUFFER ASSEMBLY

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-660	COMPLETE VFB-1000 BOARD READY TO INSTALL IN GAME	VFB-1000
52A-1-1001	CAPACITOR, CERAMIC AXIAL 150 PFD,50 VOLT, +/-20%, X7R OR Y5P	C5,C40,C64
52A-1-1002	CAPACITOR,CERAMIC AXIAL .01 MFD,50 VOLT,+/-10% Z5U	C3,C4,C6-C8,C16-C19, C25-C29,C35-C39,C46-C63,C65,C67-C76,C78-C81,C83-C87,C89-C99 C101-C105
52A-1-1003	CAPACITOR, CERAMIC, AXIAL 0.1 MFD, 50 VOLT, +80-20%	C1,C2,C9-C15,C20-C24 C30-C34,C41-C45
52C-3-1001	CAPACITOR, LYTIC, AXIAL 22 MFD, 16 VOLT, +50-10%	C77,C82,C88,C100, C106
52C-3-1002	CAPACITOR, LYTIC, AXIAL 470 MFD, 16 VOLT, +80-20%	C66
56A-1-LS00	INTEGRATED CIRCUIT (74LS00) QUAD 2 INPUT NAND GATE	1F, 5G, 7B
56A-1-7401	INTEGRATED CIRCUIT (7401) QUAD 2 INPUT NAND GATE, OPEN COLLECTOR	2D,5C,12A,12B
56A-LS02	INTEGRATED CIRCUIT (74LS02) QUAD 2 INPUT NOR GATE	1E, 5F
56A-1-LS04	INTEGRATED CIRCUIT (74LS04) HEX INVERTER	3H
56A-1-LS08	INTEGRATED CIRCUIT (74LS08) QUAD 2 INPUT AND GATE	2F
56A-1-LS10	INTEGRATED CIRCUIT (74LS10) TRIPLE 3 INPUT NAND GATE	1D,3F
56A-1-LS14	INTEGRATED CIRCUIT (74LS14) HEX SCHMITT TRIGGER	7E
56A-1-LS27	INTEGRATED CIRUIT (74LS27) TRIPLE 3 INPUT NOR GATE	5E
56A-1-LS32	INTEGRATED CIRCUIT (74LS32) QUAD 2 INPUT OR GATE	2E

56A-1-LS74	INTEGRATED CIRCUIT (74LS74) DUAL D POSITIVE-EDGE-TRIGGERED	1G,3D,4E
56A-1-LS75	INTEGRATED CIRCUIT (74LS75) 4-BIT BI-STABLE LATCH	10D, 11D
56A-1-LS109	INTEGRATED CIRCUIT (74LS109) DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR	2G, 3E, 6B
56A-1-LS153	INTEGRATED CIRCUIT (74LS153) DUAL 4-TO 1-LINE DATA SELECTORS/MULTIPLEXERS	6E,6F,6G,6H,7A,8A 8B,9A,9B,10A,10B, 11A,11B
56A-1-LS155	INTEGRATED CIRCUIT (74LS155) DUAL 2-TO 4-LINE DECODERS/DEMULTIPLEXERS	4D
56A-1-LS161	INTEGRATED CIRCUIT (74LS161) SYNCHRONOUS 4-BIT COUNTERS	3G,4G,4H,5H
56A-1-LS166	INTEGRATED CIRCUIT (74LS166) 8-BIT PARALLEL IN/SERIAL OUT SHIFT REGISTERS	9C
56A-1-LS181	INTEGRATED CIRCUIT (74LS181) ARITHMETIC LOGIC UNIT/FUNCTION GENERATORS	10C, 12C
56A-1-LS244	INTEGRATED CIRCUIT (74LS244) OCTAL THREE-STATE BUFFER	4C,5B,6A,6D
56A-1-LS273	INTEGRATED CIRUIT (74LS273) OCTAL D-TYPE FLIP-FLOP WITH CLEAR	6C, 7C
56A-1-LS367	INTEGRATED CIRUIT (74LS367) HEX BUS DRIVERS WITH THREE STATE OUTPUTS	1H
56A-6-SOO1	INTEGRATED CIRCUIT (4027-6) 4096-BIT DYNAMIC RANDOM ACCESS MEMORY	9E,9F,9G,9H,10E, 10F,10G,10H,11E, 11F,11G,11H,12E, 12F,12G,12H
25A-5-04-472	RESISTOR 4.7K OHM, 1/4 WATT, 5%	R29-R36,R45-R52,R62-R69,R74
8C-224	QUAD DIP SWITCH	2B
25A-5-04-47P	RESISTOR, 47 OHM, 1/4 WATT, 5%	R17
25A-5-04-82P	RESISTOR, 82 OHM, 1/4 WATT, 5%	R1 THRU R8
25A-5-04-221	RESISTOR, 220 OHM, 1/4 WATT,5%	R16,R21-R28,R37 -R44,R54-R61,R71 R76

25A-5-04-471	RESISTOR,470 OHM,1/4 WATT, 5%	R19, R20, R72
25A-5-04-681	RESISTOR, 680 OHM, 1/4 WATT, 5%	R11, R18
25A-5-04-102	RESISTOR, 1K OHM, 1/4 WATT, 5%	R13-R15, R77 R86, R88-R95
25A-5-04-112	RESISTOR, 1.1K OHM, 1/4 WATT, 5%	R12
25A-5-04-132	RESISTOR 1.3K OHM, 1/4 WATT, 5%	R10
25A-5-04-222	RESISTOR, 2.2K OHM, 1/4 WATT, 5%	R53,R70,R73,R75
25A-5-04-272	RESISTOR 2.7K OHM, 1/4 WATT, 5%	R9
56A-2-3904	TRANSISTOR (2N3904) NPN SILICON 40 VOLT, 350 MW	Q1

PARTS LIST FOR
ZENTRAL PROCESSING UNIT (ASSEMBLY ZPU-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-661	COMPLETE ZPU-1000 BOARD	
55C-5-1000	BATTERY (NI-CAD)	1B
55C-3-1000	CRYSTAL 10,0 MHZ	Y1
52A-1-1000	CAPACITOR, CERAMIC, AXIAL 47 PFD, 50V., +/-20%, NPO	C30
52A-1-1001	CAPACITOR, CERAMIC, AXIAL 150 PFD, 50V., +/-20% X7R OR Y5P	C31
52A-1-1002	CAPACITOR, CERAMIC, AXIAL .01 MFD, 50V., +/-10% Z5U	C4,C5,C6,C7,C9,C10,C11 C12,C13,C14,C15,C17,C18 C19,C20,C21,C22,C23,C24 C25,C26,C27,C28,C29
52A-1-1003	CAPACITOR, CERAMIC,AXIAL 0.1 MFD, 50V., +80-20%, Z5U	C32
52C-3-1000	CAPACITOR, LYTIC, AXIAL 4.7 MFD, 25V., +75-10%	C8
52C-3-1001	CAPACITOR, LYTIC, AXIAL 22 MFD, 16V., +50-10%	C1, C2 & C3
51A-1-4734	DIODE ZENER, (IN4734A) 5.6 VOLT, 5%, 1 WATT	CR26
51A-1-4148	DIODE SILICON, (1N4148) 75 VOLT, 200MA	CR1 THRU CR25,CR27 THRU CR44, CR46
56A-1-LS00	INTEGRATED CIRCUIT (74LS00) QUAD 2 INPUT NAND GATE	7G
56A-1-LS02	INTEGRATED CIRCUIT (74LS02) QUAD 2 INPUT NOR GATE	5A
56A-1-LS04	INTEGRATED CIRCUIT HEX INVERTER (74LS04)	6A
56A-1-7406	INTEGRATED CIRCUIT (7406) HEX BUFFERS WITH OPEN COLLECTOR, HIGH VOLTAGE OUTPUT	8G
56A-1-LS08	INTEGRATED CIRCUIT (74LS08) QUAD 2 INPUT AND GATE	3A

56A-1-LS20	INTEGRATED CIRCUIT (74LS20) DUAL 4-INPUT NAND GATE	4A
56A-1-LS32	INTEGRATED CIRCUIT (74LS32) QUAD 2 INPUT OR GATE	2A
56A-1-7474	INTEGRATED CIRCUIT (7474) DUAL D POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR	8A
56A-1-LS155	INTEGRATED CIRCUIT (74LS155) DUAL 2 TO 4 LINE DECODERS/DEMULT- IPLEXERS	6E & 7E
56A-1-LS244	INTEGRATED CIRCUIT (74LS244) OCTAL THREE-STATE BUFFER	5E, 6B & 7D
56A-1-LS245	INTEGRATED CIRCUIT (74LS245) OCTAL BUS TRANSCEIVER	3E
56A-1-LS367	INTEGRATED CIRCUIT (74LS367) HEX BUS DRIVERS WITH THREE STATE OUTPUTS	7A
56A-1-S001	INTEGRATED CIRCUIT (Z80) MICROPROCESSOR	7B
56A-6-2114	INTEGRATED CIRCUIT (2114) RANDOM ACCESS MEMORY 1024 X 4 BIT STATIC	2E
56A-6-S002	INTEGRATED CIRCUIT 1024 X 4 BIT RANDOM ACCESS MEMORY (COMPLETELY ACTIVE)	1E
56A-6-S004	INTEGRATED CIRCUIT 512 X 4 BIT RANDOM ACCESS MEMORY (UPPER HALF ACTIVE)	1E
56A-6-S003	INTEGRATED CIRCUIT 512 X 4 BIT RANDOM ACCESS MEMORY (LOWER HALF ACTIVE)	1E

25A-5-04-47P	RESISTOR, 47 OHM, 1/4 WATT, 5%	R32 & R42
25A-5-04-101	RESISTOR, 100 OHM, 1/4 WATT 5%	R18, R66
25A-5-04-271	RESISTOR, 270 OHM, 1/4 WATT 5%	R29
25A-5-04-391	RESISTOR, 390 OHM, 1/4 WATT 5%	R44 & R68
25A-5-02-471	RESISTOR, 470 OHM, 1/2 WATT,5%	R36
25A-5-04-102	RESISTOR, 1K OHM, 1/4 WATT 5%	R31,R48,R50,R51,R54, R55,R64,R65
25A-5-04-222	RESISTOR, 2.2K OHM, 1/4 WATT 5%	R1,R10-R17,R28 R33,R35 & R40
25A-5-04-472	RESISTOR, 4.7 K OHM, 1/4 WATT 5%	R2-R9,R67
25A-5-04-822	RESISTOR, 8.2K OHM, 1/4 WATT 5%	R30 & R37
25A-5-04-103	RESISTOR, 10K OHM, 1/4 WATT,5%	R20-R27,R59-R63 R43,R58,R69
25A-5-04-203	RESISTOR, 20K OHM, 1/4 WATT,5%	R38 & R41
25A-5-04-473	RESISTOR, 47K OHM,1/4 WATT, 5%	R19,R39,R45,R46,R47, R49,R52,R53,R56, R57
25A-5-04-124	RESISTOR, 120K OHM,1/4 WATT,5%	R34
8C-225	SWITCH, DIP 8 POSITION	2F,3F,4F,5F & 6F
8C-226	SWITCH, PUSH BUTTON	SW1 & SW2
51A-2-S001	L.E.D.	CR45
50A-4-1003	STAND-OFF (FOR CR45)	
53A-2-3904	TRANSISTOR, (2N3904) NPN SILICON 40 VOLT, 350 MW	Q1, Q2 & Q5
53A-1-4403	TRANSISTOR, (2N4403) PNP SILICON 40 VOLT, 350 MW	Q3,Q4,Q6 THRU Q11
53A-1-0137	TRANSISTOR,(TIS137) PNP SILICON 35 VOLT, 625 MW	Q12

PARTS LIST FOR
SOUND BOARD (ASSEMBLY SB-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-665	COMPLETE SB-1000 BOARD	
52A-1-1004	CAPACITOR, CERAMIC, AXIAL 820 PFD, 50 VOLT, +/-10%, Z5U	C14
52A-1-1005	CAPACITOR, CERAMIC, AXIAL.0033 MFD,25 VOLT, +/-20%, Z5U	C25
52A-1-1002	CAPACITOR, CERAMIC, AXIAL .01 MFD, 50 VOLT, +/-10%, Z5U	C1,C5,C6,C7,C9,C10, C18,C19,C21,C22,C26, C28,C29,C30,C31,C32, C34
52A-1-1003	CAPACITOR, CERAMIC, AXIAL .1 MFD, 50 VOLT, +80-20%, Z5U	C8,C15,C20,C27,C33
52A-3-1000	CAPACITOR,LYTIC, AXIAL 4.7 MFD, 25 VOLT, +75-10%	C2,C3,C4,C11,C12, C13,C35
52C-3-1003	CAPACITOR, LYTIC, AXIAL 47 MFD, 16 VOLT, +80-20%	C16
52C-3-1002	CAPACITOR, LYTIC, AXIAL 470 MFD, 16 VOLT,+80-20%	C17, C24
52C-3-1004	CAPACITOR, LYTIC, AXIAL 1000 MFD, 25 VOLT, +80-20%	C23
A-605-HS	HEAT SINK & POWER AMPLIFIER SUB-ASS'Y	C8
56A-1-6840	INTEGRATED CIRCUIT 6840 PROGRAMMABLE TIMER	A1
56A-1-7401	INTEGRATED CIRCUIT 7401 QUAD 2 INPUT NAND GATE OPEN COLLECTOR	A9
56A-1-LS04	INTEGRATED CIRCUIT (74LS04) HEX INVERTER	7B
56A-1-LS08	INTEGRATED CIRCUIT (74LS08) QUAD 2 INPUT AND GATE	9B
56A-1-LS74	INTEGRATED CIRCUIT (74LS74) DUAL D,POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR	8B,9C,10C
56A-1-LS86	INTEGRATED CIRCUIT (74LS86) QUAD TWO INPUT EXOR	8A

56A-1-LS139	INTEGRATED CIRCUIT (74LS139) DUAL 2 TO 4 LINE DECODER	6A
56A-1-4562	INTEGRATED CIRCUIT (4562B) 128-BIT SHIFT REGISTER	7A
56A-1-4051	INTEGRATED CIRCUIT (4051B) 8 CHANNEL ANALOG MULIPLEXER	2B,3B,4B
56A-1-4053	INTEGRATED CIRCUIT (4053B) TRIPLE 2 CHANNEL ANALOG MULTIPLEXER	6B,2C
56A-1-4175	INTEGRATED CIRCUIT (4175B) QUAD D-TYPE FLIP-FLOP	2A,3A,4A 5A
56A-2-3340	INTEGRATED CIRCUIT (3340P) ELECTRONIC ATTENUATOR	3C
56A-2-2002	INTEGRATED CIRCUIT (TDA2002AV) POWER AMPLIFIER	
25A-5-04-2P2	RESISTOR, 2.2 OHM,1/4 WATT,5%	R20,R24
25A-5-04-3P9	RESISTOR, 3.9 OHM, 1/4 WATT,5%	R1,R2
25A-5-04-7P5	RESISTOR, 7.5 OHM, 1/4 WATT,5%	R19
25A-5-04-16P	RESISTOR, 16 OHM, 1/4 WATT,5%	R18
25A-5-04-33P	RESISTOR, 33 OHM, 1/4 WATT,5%	R16
25A-5-04-68P	RESISTOR, 68 OHM, 1/4 WATT,5%	R17
25A-5-04-131	RESISTOR, 130 OHM, 1/4 WATT,5%	R15
25A-5-04-221	RESISTOR, 220 OHM, 1/4 WATT,5%	R27
25A-5-04-271	RESISTOR, 270 OHM, 1/4 WATT,5%	R14
25A-5-04-471	RESISTOR, 470 OHM, 1/4 WATT,5%	R23
25A-5-04-472	RESISTOR, 4.7K OHM, 1/4 WATT,5%	R3,R4,R5 R6,R7,R8 R9,R11,R12 R13,R22 R25,R26 R28
25A-5-04-103	RESISTOR, 10K OHM, 1/4 WATT,5%	R10,R21

PARTS LIST FOR
POWER SUPPLY ASSEMBLY (PS-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-668	POWER SUPPLY ASSEMBLY, COMPLETE	
50B-4-1001	BUSHING, NYLON INSULATING (B51547F015) (USED ON VR3)	
52A-1-1002	CAPACITOR, CERAMIC, AXIAL .01 MFD, 500 10% Z5U	C5,C7,C9
52C-3-1001	CAPACITOR, LYTIC AXIAL 22 MFD, 16V., +50-10%	C4,C6,C8,C10
52C-3-1005	CAPACITOR LYTIC 1000 MFD, 35V., +80-20%	C3
52C-3-1006	CAPACITOR, LYTIC 6800 MFD, 35V., +80-20%	C2
52G-3-1007	CAPACITOR, LYTIC 15,000 MFD, 16V., +80-20%	C1
8B-159	FUSE CLIP	F1,F2,F3
8A-157-P75	FUSE 3/4 AMP, 250 VOLT, 3 AG (SLO-BLOW)	F2
8A-111-3	FUSE 3 AMP, 125 VOLT, 3 AG (SLO-BLOW)	F1
8A-111-5	FUSE 5 AMP, 125 VOLT, 3 AG	F3
50D-2H-6	HEAT SINK (THERMALLOY #6033-43-43-43-43)	
51A-1-5391	RECTIFIER, SILICON 50 VOLT, 1.5 AMP (IN5391)	CR5,CR6,CR7,CR8
51A-1-S001	RECTIFIER, SILICON (MR500) 50 VOLT 3 AMP	CR1,CR2,CR3,CR4
56A-5-7812	REGULATOR (7812) 12 VOLT, 1 AMP.	VR1
56A-5-7815	REGULATOR, (7815) 15 VOLT, 1 AMP.	VR2
56A-5-7905	REGULATOR, (7905) -5 VOLT, 1 AMP.	VR3
25A-9-5-5P6	RESISTOR,5.6 OHM, 5 WATT, 20% W.W.	R4
25A-5-04-12P	RESISTOR, 12 OHM, 1/4 WATT, 5%	R1
25A-9-5-13P	RESISTOR, 13 OHM, 5 WATT, 10%W.W.	R5
25A-5-04-121	RESISTOR, 120 OHM, 1/4 WATT, 5%	R2
25C-16-5	POTENTIOMETER, 1K OHM TRIMMER	R3

PARTS LIST FOR
VOICE SYNTHESIZER UNIT (ASSEMBLY VSU-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-708	COMPLETE VSU-1000 BOARD	
	VOICE PROGRAMED PROM (SEE GAME MANUAL)	1C,2C
52A-1-1001	CAPACITOR, CERAMIC, AXIAL 150 PFD, 50V., +/-20%, X7R OR Y5P	C23
52A-1-1002	CAPACITOR, CERAMIC, AXIAL .01 MFD, 50V., +/-10%, Z5U	C1,C3,C5,C12,C17,C19 C20,C21,
52A-1-1007	CAPACITOR, CERAMIC, AXIAL .022 MFD, 25V., +/-20%, X7R	C24
52A-1-1003	CAPACITOR, CERAMIC, AXIAL .1 MFD, 50V. +/-20%, Z5U	C4,C18,C22
52A-1-1008	CAPACITOR, CERAMIC, AXIAL .27 MFD, 25V., +/-20%, Z5U	C16
52C-3-1000	CAPACITOR, LYTIC, AXIAL 4.7 MFD., 25V., +75-10%	C14
52C-3-1001	CAPACITOR, LYTIC AXIAL 22 MFD, 16V., +50-10%	C15
52C-3-1002	CAPACITOR, LYTIC, AXIAL 470MFD,16V, +80-20%	C2,C13
51A-1-4148	DIODE, SILICON (1N4148) 75 VOLT, 200 MA	CR2,CR3
51A-1-4740	ZENER DIODE (1N4740A) 10 VOLT, 1 WATT	CR1
56A-1-7401	INTEGRATED CIRCUIT (7401) QUAD 2 INPUT NAND GATE OPEN COLLECTOR	2A
56A-1-LS04	INTEGRATED CIRCUIT (74LS04) HEX INVERTER	4A
56A-1-LS27	INTEGRATED CIRCUIT (74LS27) TRIPLE 3 INPUT NOR GATE	1A
56A-1-LS139	INTEGRATED CIRCUIT (74LS139) DUAL 2 TO 4 LINE DECODER	3A
56A-1-LS161	INTEGRATED CIRCUIT (74LS161) SYNCHRONOUS 4-BIT COUNTER	5A,6A

56A-1-4174	INTEGRATED CIRCUIT (14174B) HEX D FLIP-FLOP	5B,6B
56A-2-0555	INTEGRATED CIRCUIT (555) TIMER	2B
56A-2-1458	INTEGRATED CIRCUIT (1458) DUAL OP. AMP	5C
56A-1-4051	INTEGRATED CIRCUIT (4051B) 8 CHANNEL ANALOG MULTIPLEXER	6C
56A-3-S001	INTEGRATED CIRCUIT (CUSTOM ROM CONTROLLER/CRC) (T.S.I.)	3C
25A-5-04-101	RESISTOR, 100 OHM, 1/4 WATT, 5%	R20
25A-5-2-201	RESISTOR, 200 OHM, 2 WATT, 5%	R1
25A-5-04-391	RESISTOR, 390 OHM, 1/4 WATT, 5%	R2,R3
25A-5-04-561	RESISTOR, 560 OHM, 1/4 WATT, 5%	R23
25A-5-04-751	RESISTOR, 750 OHM, 1/4 WATT, 5%	R22
25A-5-04-102	RESISTOR, 1K OHM, 1/4 WATT, 5%	R19,R25
25A-5-04-132	RESISTOR, 1.3K OHM, 1/4 WATT, 5%	R24
25A-5-04-152	RESISTOR, 1.5K OHM, 1/4 WATT, 5%	R21
25A-5-04-222	RESISTOR, 2.2K OHM, 1/4 WATT, 5%	R4,R11,R12,R13,R14 R26
25A-5-04-302	RESISTOR, 3.0K OHM, 1/4 WATT, 5%	R27
25A-5-04-103	RESISTOR, 10K OHM, 1/4 WATT, 5%	R34,R35,R36
25A-5-04-183	RESISTOR, 18K OHM, 1/4 WATT, 5%	R10
25A-5-04-273	RESISTOR, 27K OHM, 1/4 WATT, 5%	R33
25A-5-04-104	RESISTOR, 100K OHM, 1/4 WATT, 5%	R5,R6,R7,R8,R9 R15,R16,R17
25A-5-04-244	RESISTOR, 240K OHM, 1/4 WATT, 5%	R18,R29,R30,R32 R37
25A-5-04-274	RESISTOR, 270K OHM, 1/4 WATT, 5%	R28,R31

PARTS LIST FOR
HEAT SINK ASSEMBLY

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-704	COMPLETE ASSEMBLY	
50D-3-1002	HEAT SINK (THERMALLOY 6421B-2, WAKEFIELD 421)	
50B-4-1002	INSULATOR, REINFORCED SILICONE	
50C-2-1000	TO-3 SOCKET (THERMALLOY 8113-PF-603)	
50A-5-S001	REGULATOR, 5 VOLT, 3 AMPERE	
52A-1-1003	CAPACITOR, AXIAL .1 MFD, 50 VOLT, +80-20%, Z5U	

PARTS LIST
FOR
BUFFER SYSTEM COLOR ASSEMBLY (BSC-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-766	COMPLETE ASSEMBLY: READY TO INSTALL	
52A-1-1002	CAPACITOR, CERAMIC, AXIAL .01 MFD, 50V., +/-10%, Z5U	C1,C2,C3,C4,C5,C7-C19
52C-3-1001	CAPACITOR, LYTIC AXIAL 22 MFD, 16V., +50-10%	C6
56A-1-LS00	INTEGRATED CIRCUIT (74LS00) QUAD 2 INPUT NAND GATE	C1, D2
56A-1-7401	INTEGRATED CIRCUIT (7401) QUAD 2 INPUT NAND GATE OPEN COLLECTOR	F1
56A-1-LS04	INTEGRATED CIRCUIT (74LS04) NEX INVERTER	D1
56A-1-7406	INTEGRATED CIRCUIT,(7406) HEX BUFFERS WITH OPEN COLLECTOR, HIGH VOLTAGE OUTPUT	E3
56A-1-LS10	INTEGRATED CIRCUIT (74LS10) TRIPLE 3 INPUT NAND GATE	D3
56A-1-LS27	INTEGRATED CIRCUIT (74LS27) TRIPLE 3 INPUT NOR GATE	1E
56A-1-LS74	INTEGRATED CIRCUIT (74LS74) DUAL D POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR	2E
56A-1-LS245	INTEGRATED CIRCUIT (74LS245) OCTAL BUS TRANSCEIVER	3A
56A-1-LS257	INTEGRATED CIRCUIT (74LS257) QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS	4A,4B,3C,4C
56A-1-LS273	INTEGRATED CIRCUIT (74LS273) OCTAL D-TYPE FLIP-FLOP WITH CLEAR	2C
56A-6-2114	INTEGRATED CIRCUIT (2114) (1024 X 4 BIT STATIC RANDOM ACCESS MEMORY	2A,1B,2B,3B
25A-5-04-82P	RESISTOR, 82 OHM, 1.4 WATT, 5%	R4,R5,R6,R7,R8,R9,R10, R11
25A-5-04-271	RESISTOR, 270 OHM, 1/4 WATT, 5%	R16,R17,R18

25A-5-04-361	RESISTOR, 360 OHM, 1/4 WATT, 5%	R19,R20,R21
25A-5-04-391	RESISTOR, 390 OHM, 1/4 WATT, 5%	R1,R3,R12
25A-5-04-751	RESISTOR, 750 OHM, 1/4 WATT, 5%	R13,R14,R15
25A-5-04-103	RESISTOR, 10K OHM, 1/4 WATT, 5%	R2
8C-224	SWITCH, QUAD	F2

PARTS LIST
FOR
RESISTOR CAPACITOR ASSEMBLY (RCR-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-788	RCR-1000 ASSEMBLY: READY TO INSTALL	
52A-1-1006	CAPACITORS, CERAMIC AXIAL .001 MFD. 50V., +/-10%, Y5P	C1 THRU C13, C16 THRU C30,C32
52A-1-1001	CAPACITOR, CERAMIC AXIAL 150 PFD, 50V., +/-20%, X7P OR Y5P	C14,C15,C31
25A-5-04-10P	RESISTOR, 10 OHM, 1/4 WATT, 5%	R1 THRU R54

PARTS LIST FOR PHOTO REFLECTIVE UNIT (PRU-1000)

STERN PART NO.	DESCRIPTION	REFERENCE DESIGNATION
A-719	COMPLETE ASS'Y	PRU-1000
52A-1-1003	CAPACITOR, AXIAL, CERAMIC 0.1 MFD, 50V, +80-20% Z5U	C1,C2
52C-3-1001	CAPACITOR, AXIAL, LYTIC 22 MFD, 16V., +50-10%	C3
56A-2-0339	INTEGRATED CIRCUIT (QUAD CAMPARATOR) (LM339)	U1
55A-1-1000	REFLECTIVE OBJECT SENSOR (TRW-OPTON OPB 707A)	U2,U3,U4,U5
25A-5-04-101	RESISTOR 100 OHM,1/4 WATT,5%	R1,R4,R9,R10
25A-5-04-221	RESISTOR 220 OHM,1/4 WATT,5%	R5,R6,R7,R8
25A-5-04-242	RESISTOR 2.4K OHM,1/4 WATT,5%	R2
25A-5-04-682	RESISTOR 6.8K OHM,1/4 WATT,5%	R3

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