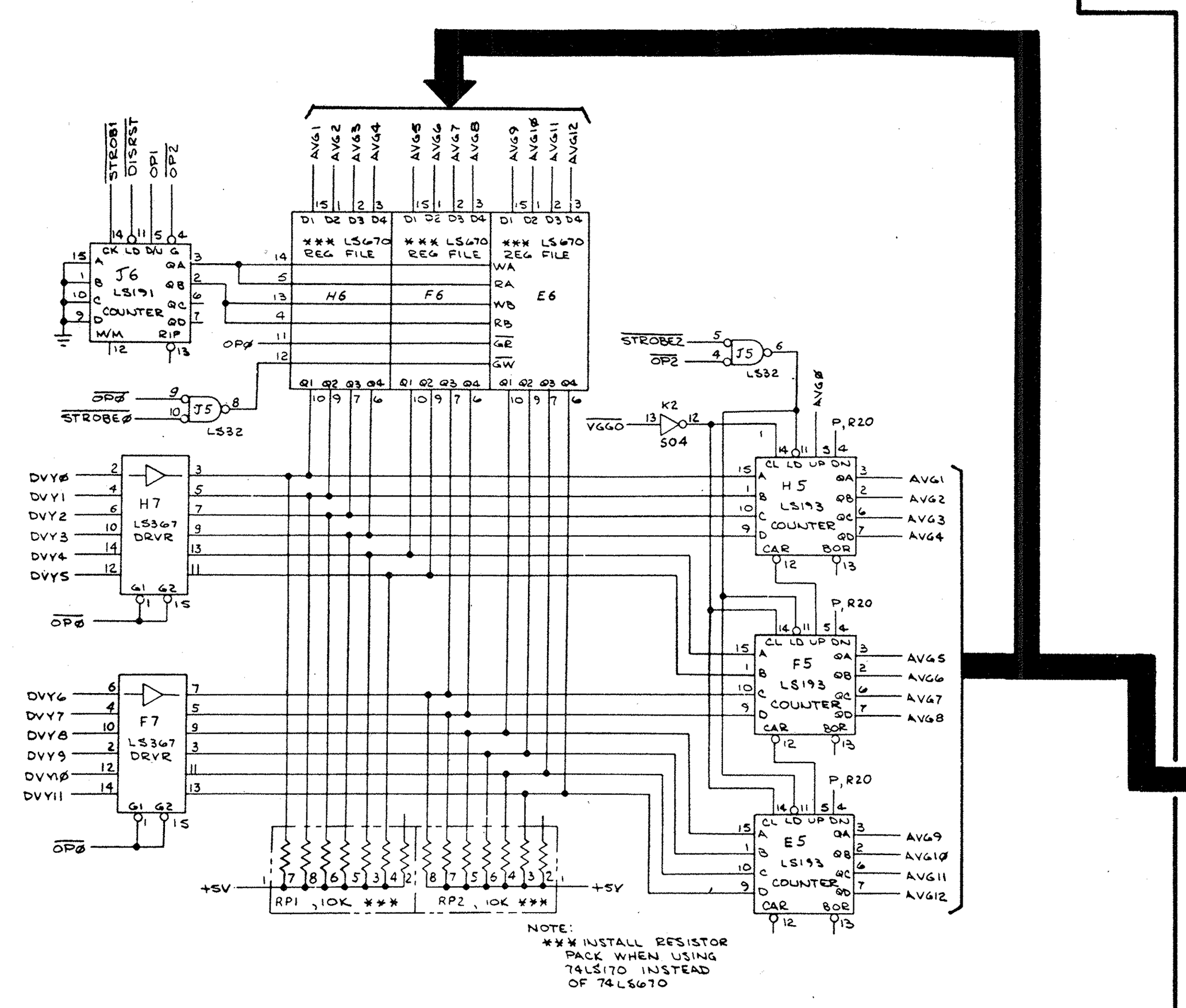
Stack and Program Counter



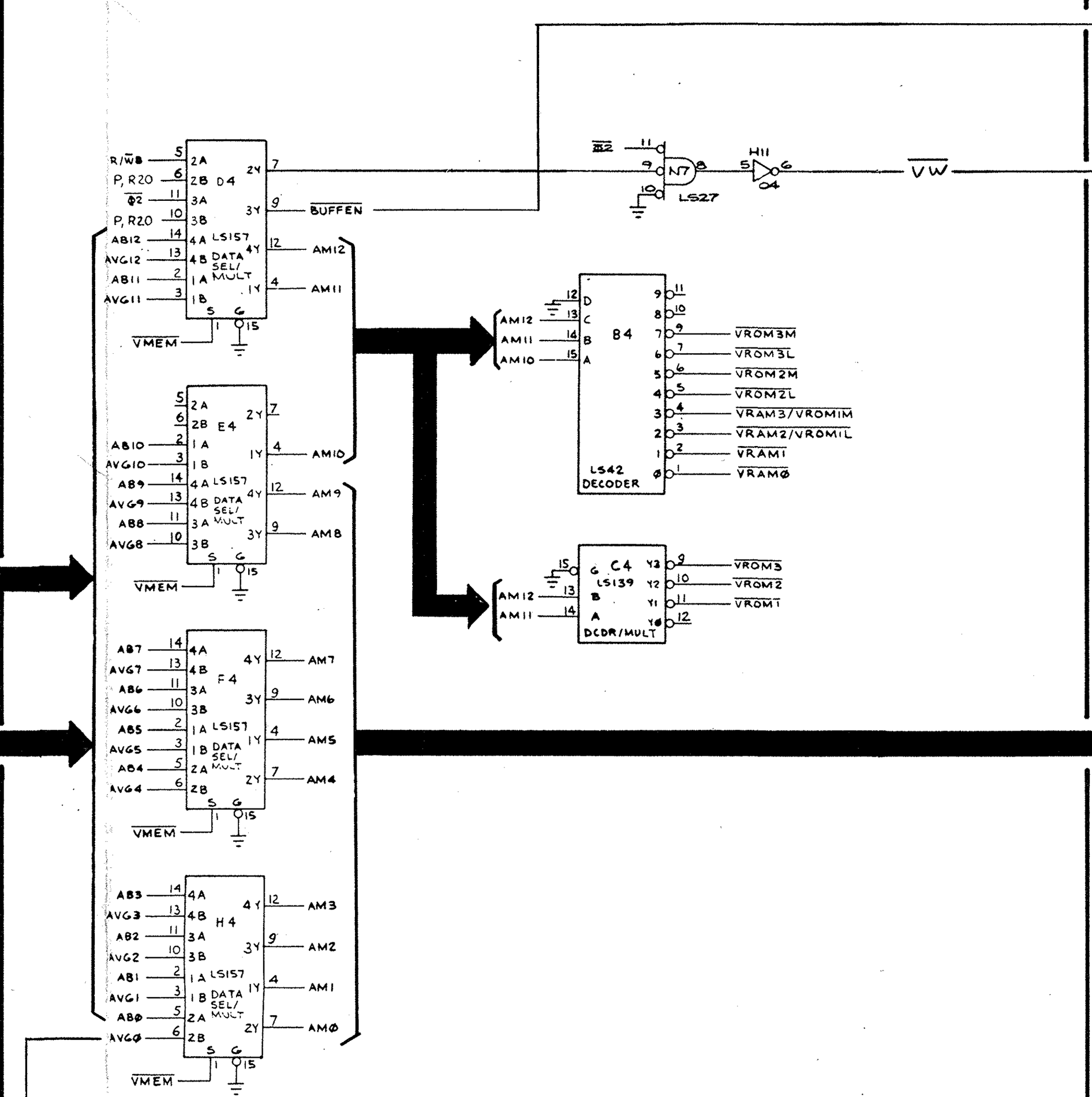
The Stack and Program Counter circuitry consists of counters E5, F5,H5 and J6, buffers F7 and H7, file registers E6, F6, H6, and associated gates. Counter J6 and file registers E6, F6, and H6 make up the stack circuit. The program counter increments one count (to the next sequential address) each time AVG0 goes high. Counters E5, F5 and H5 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter.

The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data shift registers C5, D5, and D6, and program-counter buffers F7 and H7.

The program counter can also be preset to "return" to a previous address which it had stored in its "stack". The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when STROBE 1 goes high. Immediately after information is written into the stack, counter J6 increments one count. Immediately before loading the program counter from the stack, counter J6 decrements one count.

From MPU Buffered Address AB0 thru AB12

Vector-Generator Address Selector



The address selector consists of demultiplexer C4, multiplexers D4, E4, F4 and H4, and decoder B4. When $\overline{VMEM}$ is low, the MPU gains access to the address inputs of the vector-generator memory. In this state, $\overline{BUFFEN}$ is from $\overline{\Phi 2}$, and $\overline{VW}$ (vector generator write) is low when $\overline{\Phi 2}$ and $R/\overline{WB}$ are both low. When $\overline{VMEM}$ is high, the address input to the vector-generator memory is from the vector-generator program counter and state machine. In this state, $\overline{BUFFEN}$ and $\overline{VW}$ are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer D4.

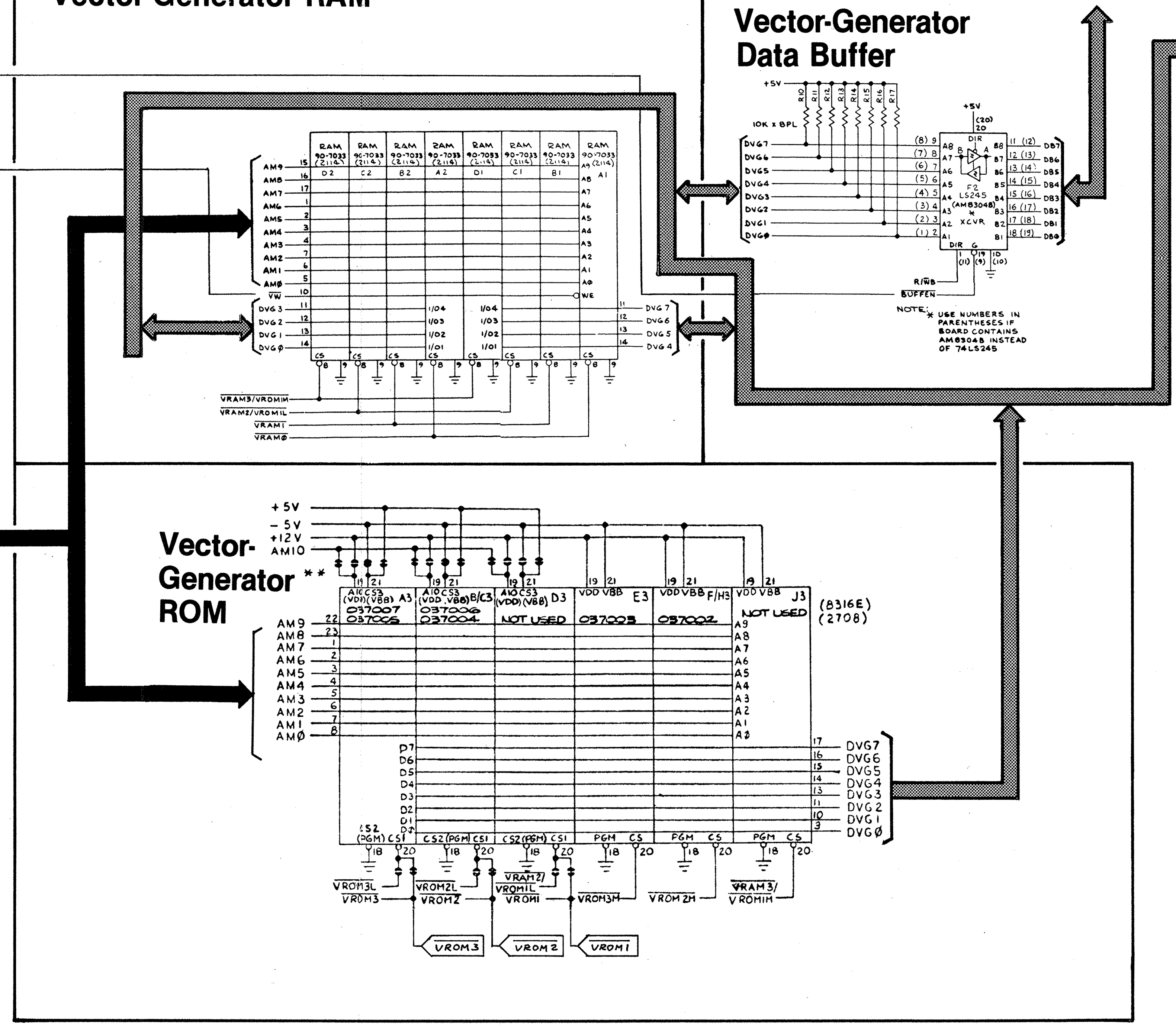
Decoder B4 and demultiplexer C4 decode address bits AM10-AM12, and select the RAM or one of two ROMs of the vector-generator memory.

This address-selecting arrangement allows the game MPU to access the vector-generator memory, (write data into the vector-generator RAM to instruct the vector generator what it should do next). The address selector can then allow the vector-generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

Vector-Generator RAM

Vector-Generator Data Buffer

Vector-Generator ROM



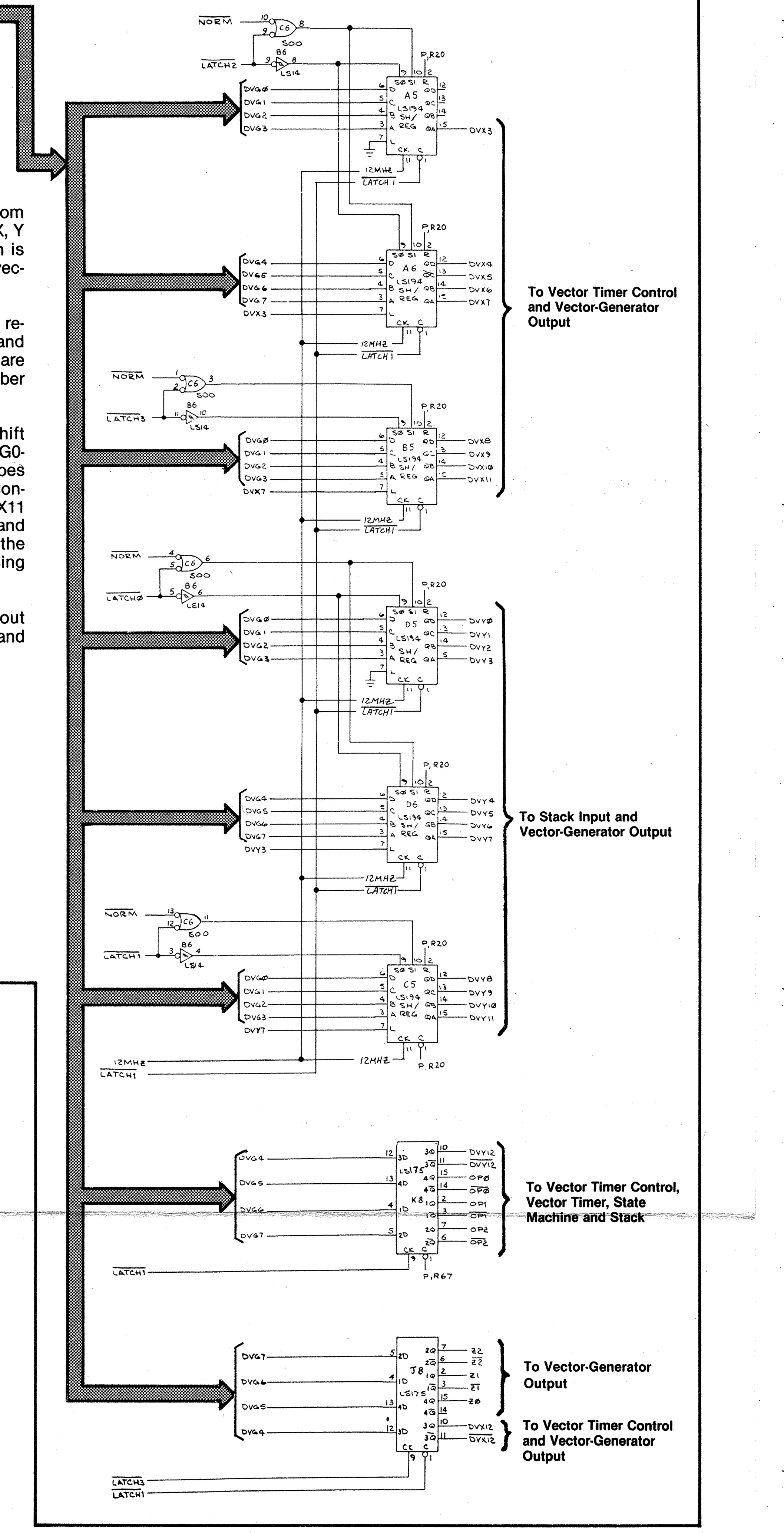
Vector Generator Data Shifter

The Vector-Generator Data Shifter receives data from the vector-generator memory circuits and generates X, Y and Z axis information. The X and Y axis information is then shifted up to decrease the drawing time of the vectors.

The Vector-Generator Data Shifter consists of shift registers A5, A6, B5, C5, D5, and D6, latches J8 and K8, and gates B6 and C6. The X and Y data shifter circuits are identical, so only the X is explained. However, remember that these circuits function at the same time.

$\overline{LATCH\ 1}$ when low clears the output of the shift registers. When $\overline{LATCH2}$ and $\overline{LATCH3}$ are low, DVG0-DVG7 is loaded into A5, A6 and B5. When $\overline{NORM}$ goes low, the information is shifted up. This operation continues until DVX11 and DVX12 are different levels (DVX11 is high and DVX12 is low or vice versa) or until DVY11 and DVY12 are different levels. This condition clears the NORM flip-flop in the Vector-timer control circuit causing the data shifter to stop.

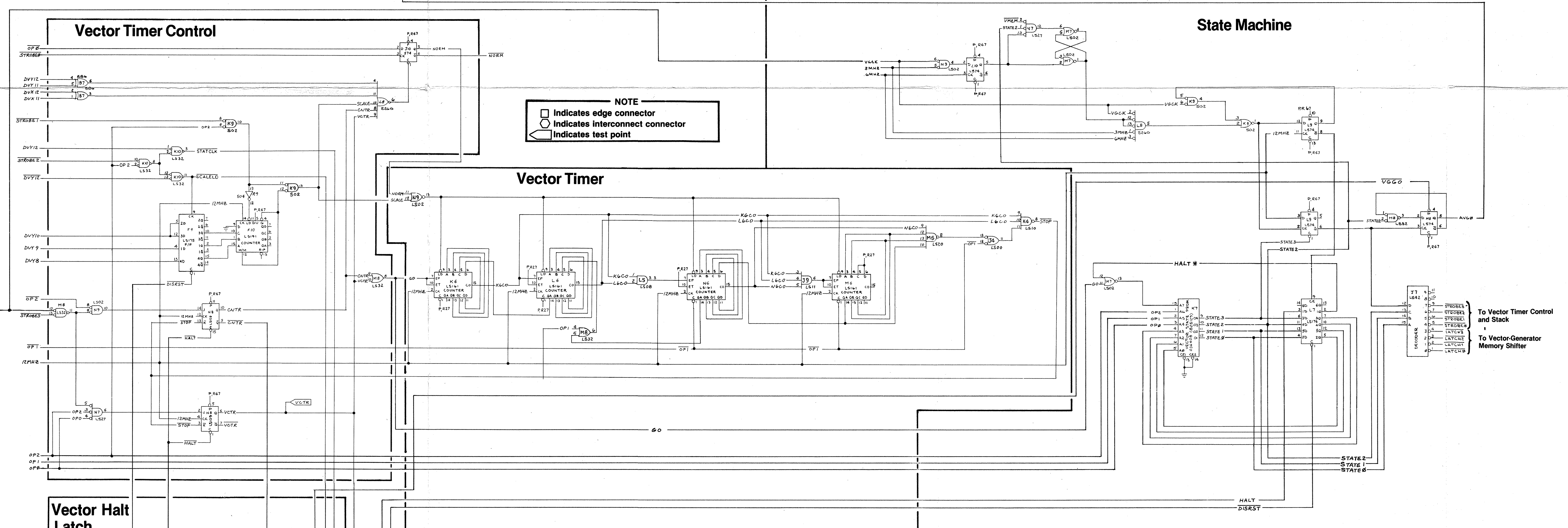
Latches J8 and K8 receive DVG4-DVG7 and latch out OP0-OP2, $\overline{OP0-OP2}$, DVX12, $\overline{DVX12}$, DVY12, $\overline{DVY12}$, and Z0-Z2 and $\overline{Z0-Z2}$.



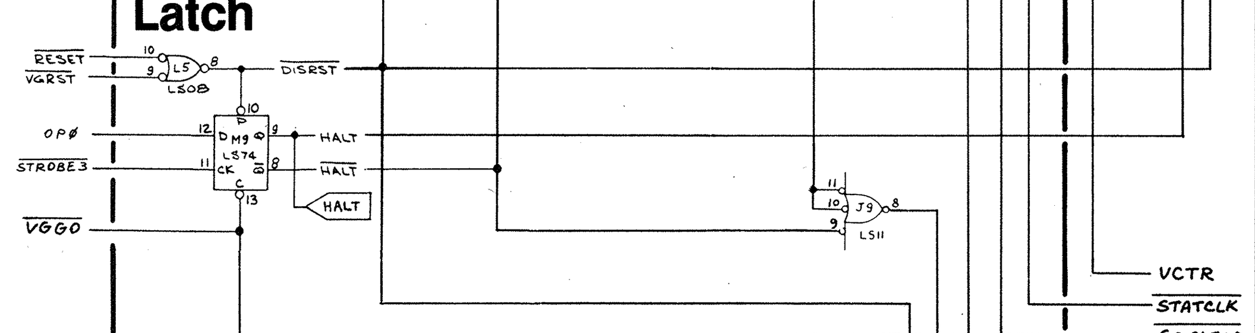
Vector Timer Control

Vector Timer

State Machine



Vector Halt Latch



Vector halt latch M9 receives OP0 from the vector-generator data shifter and a STROBE3 clock signal from the state machine. When $\overline{RESET}$ counter or $\overline{VGRST}$ from the address decoder go low at gate L5, the vector generator outputs a HALT signal that prevents a vector from being drawn. When $\overline{VGGO}$ from the address decoder goes low or when $\overline{DISRST}$ goes high, the HALT signal goes low and the state machine resumes operation.

The vector timer determines the actual time it takes to draw the vector. The vector timer consists of counters K6, L6, M6, and N6 and associated gates. When GO goes high, the vector-timer counters are enabled. When either NORM or SCALE at gate N9 are high, the output of the counter is shifted down (left).

The carry out of each counter is applied to the next counter's load input and to gates K4 and M5. When the carry out (pin 15) of all counters is high, $\overline{STOP}$ goes low and disables the vector timer via latches N8 in the vector-timer control circuity.

The state machine is the "master controller" of the vector-generator circuitry, and receives instructions from the game MPU. These instructions determine whether the state machine: 1) draws a vector; 2) moves the monitor beam to a new position on the monitor display; 3) "jumps" to a new vector memory address; 4) returns to a previous vector memory address; or 5) tells the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gate M7, vector-state PROM K7, and decoder L7. The operation codes (OP0-OP2) from the vector-generator data shifter tell PROM K7 which operation to perform. Pins 4-7 of PROM K7 receive data from latch L7 telling the PROM which operation was last performed. Pin 15 of K7, when low, tells the PROM that a vector is presently being drawn. The state machine will not proceed to its next instruction until pin 15 goes high. Pin15 goes low if a HALT* and/or GO signal are present.

The state machine decoder J7 receives $\overline{STATE0-STATE3}$ signals from the Prom and a clock signal from L9 pin 6. The output signals $\overline{STROBE0-STROBE3}$ go to the vector-timer control and stack circuitry. Signals $\overline{LATCH0-LATCH3}$ are sent to the vector-generator data shifter.

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Sheet 3, Side A

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Vector-Generator Program Counter
Vector-Generator RAM
Vector-Generator ROM
Vector-Generator Data Shifter
Vector-Generator Data Buffer
Vector-Generator Data Latches
Vector-Generator Vector Timer
Vector-Generator State Machine

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