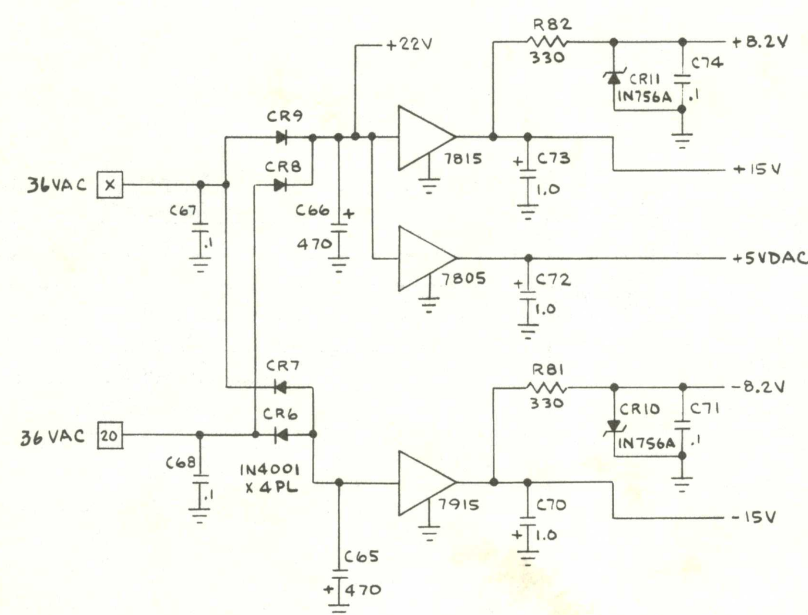
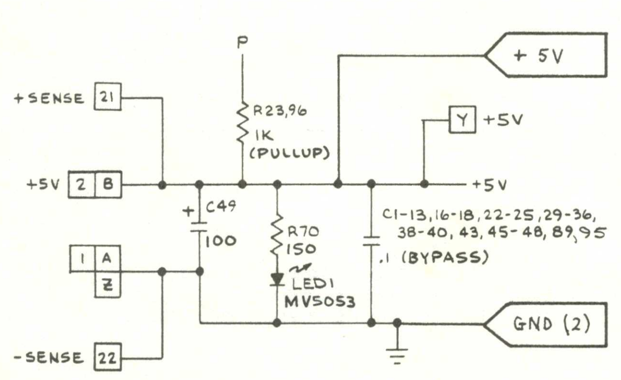
POWER INPUT



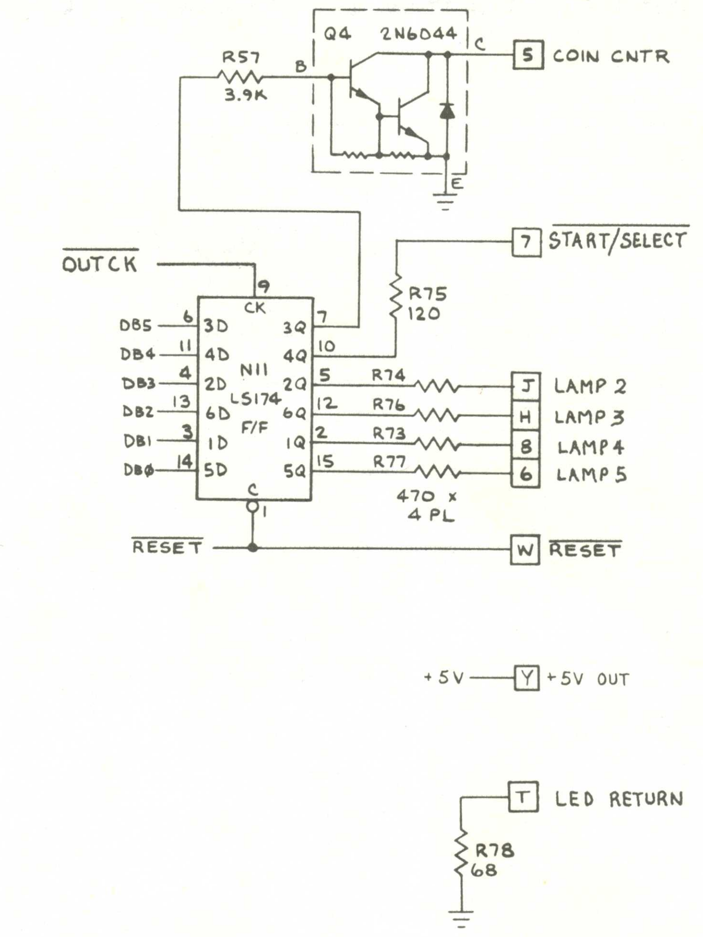


This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on the Sheet 1, Side A of this schematic set.

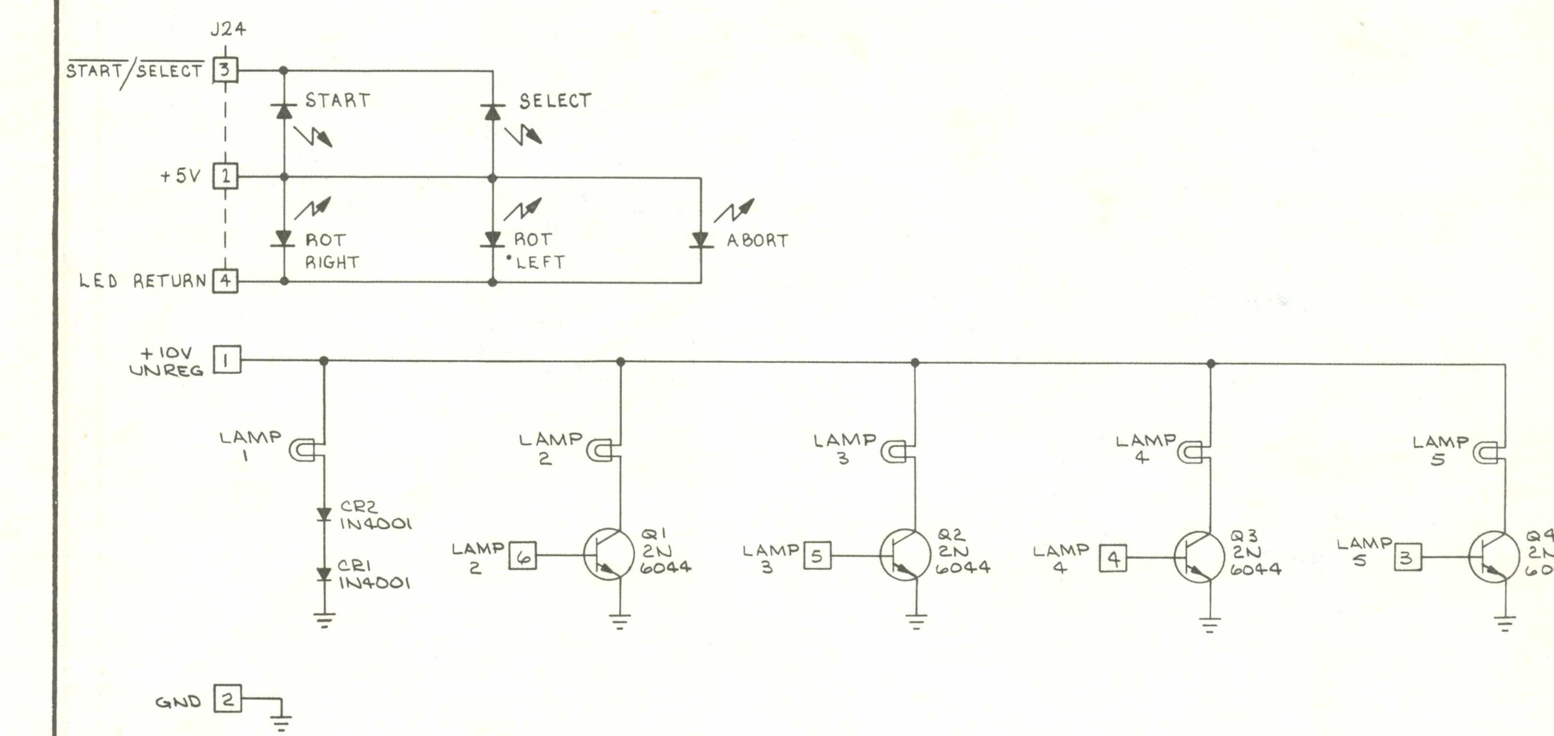
The 36 VAC inputs are received by two full wave rectifiers. Diodes CR6 and CR7 rectify the negative cycle of the input and the 7915 regulates the voltage at −15 VDC. Diodes CR8 and CR9 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR11 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifier R7 in the audio output.

LAMP, LED, AND COIN COUNTER OUTPUT

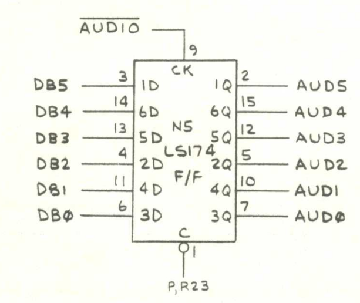
This circuit consists of coin counter driver Q4 and data latch N11, clocked by the microcomputer's address decoder. When the input to Q4 is high, the collector goes low grounding the return of the coin counter in the coin door. When START/SELECT is clocked low, it grounds the START and SELECT LEDs in the control panel. When LAMP2, LAMP3, LAMP4, or LAMP5 is clocked high the appropriate lamp driver transistor is biased into conduction lighting the lamp. LAMP2 is TRAINING MISSION, LAMP3 is CADET MISSION, LAMP4 is PRIME MISSION, and LAMP5 is the COMMAND MISSION lamp.

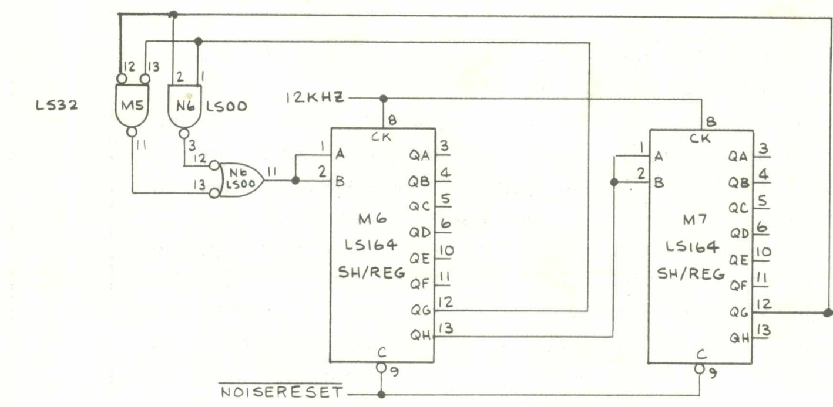


PART OF CONTROL PANEL



AUDIO OUTPUT





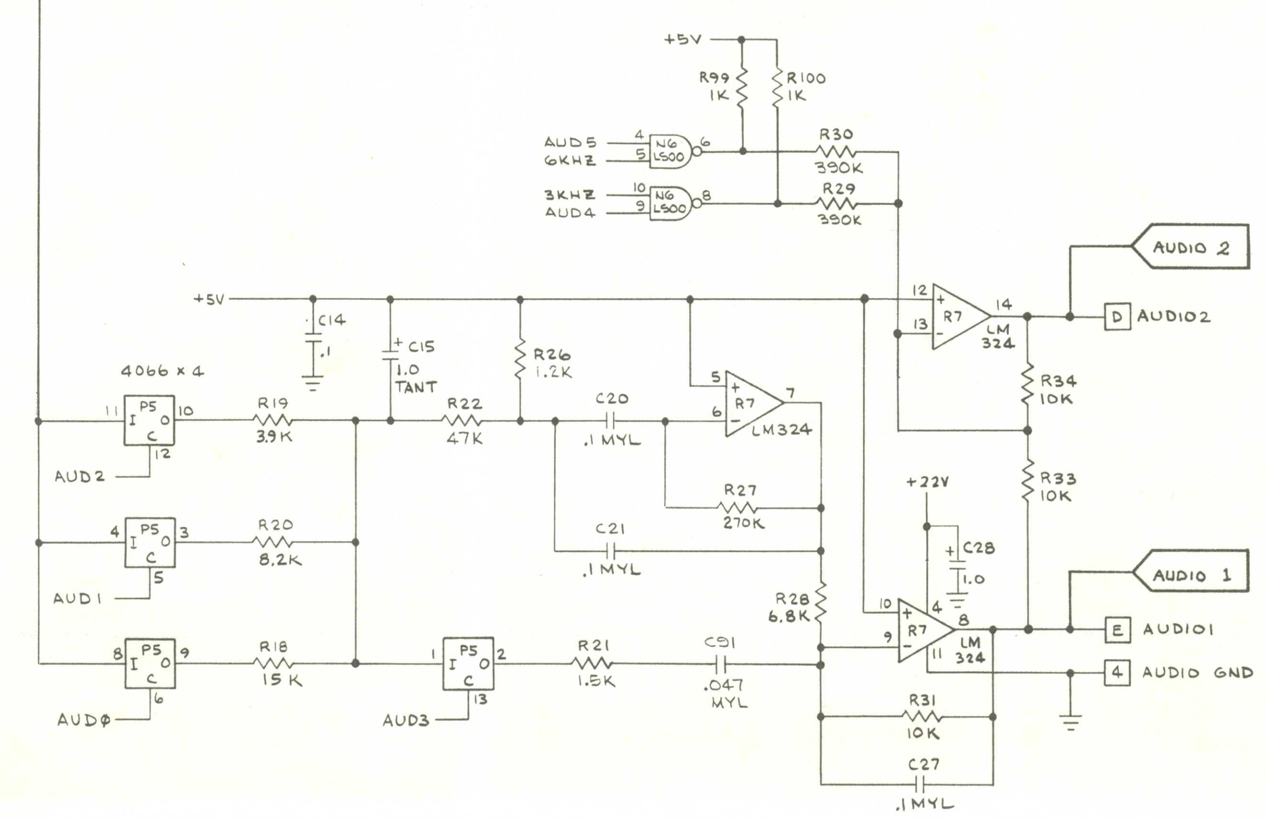
There are four sounds generated in the Lunar Lander game: thrust, explosion, 3 KHz and 6 KHz. All audio control lines are altered by the microcomputer when AUDIO, from the address decoder, is low. The enabled audio depends on the state of AUD0 thru AUD5.

Thrust and explosion audio signals are both developed by random noise from noise generator M6 and M7. The resistive and capacitive network connected to the pin 6 input of operational amplifier R7 is a low pass filter that filters out the high frequencies for the thrust audio. The pins 8 and 14 outputs of op amp R7 develop two equal amplitude, opposite phase signals for the thrust and explosion signals only. Pin 14 of R7 is the output for the 3 KHz and 6 KHz signals.

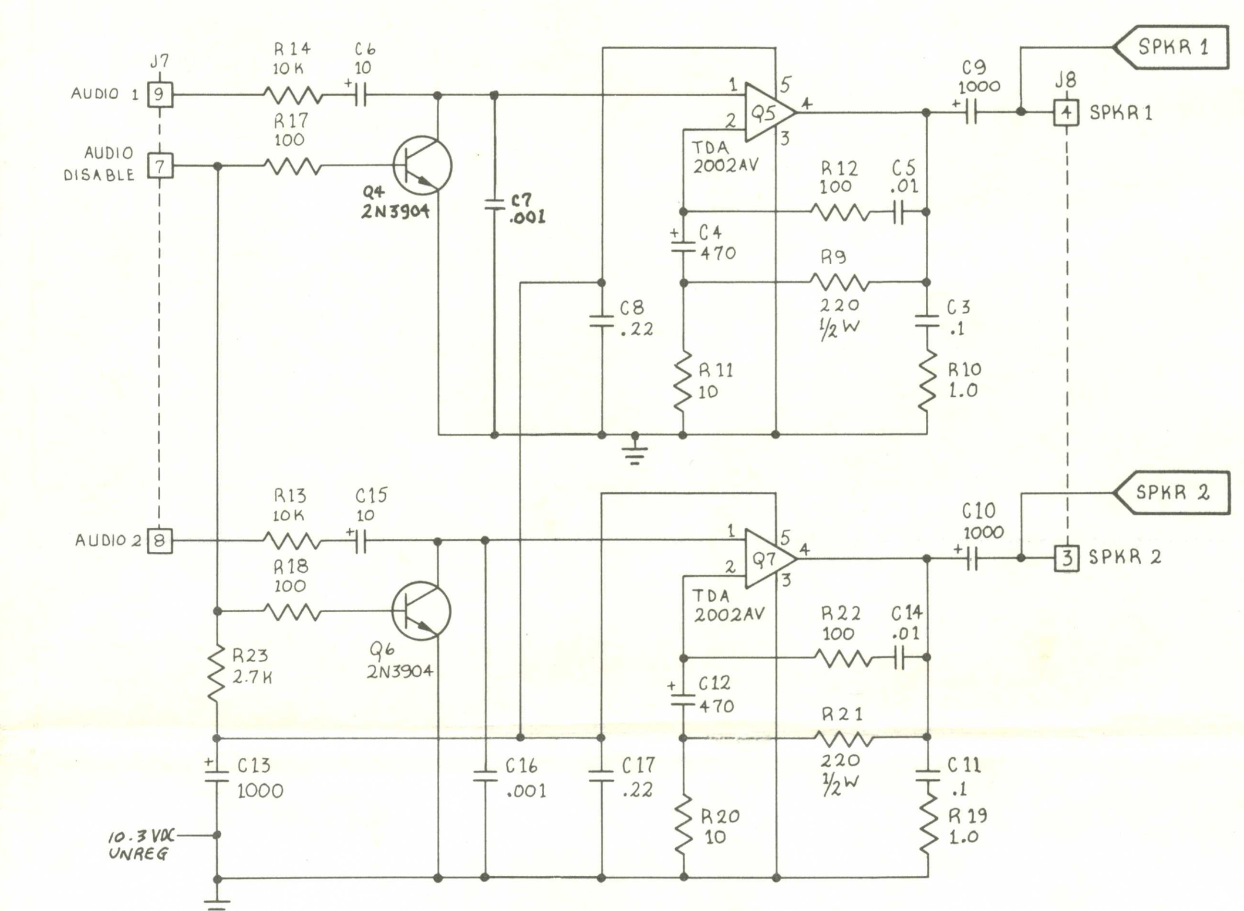
Thrust passes through analog switches P5 when AUD0 and/or AUD1, and/or AUD2 is high. When AUD0 only is high, the thrust audio is at its lowest volume. When AUD0 thru AUD2 are all high, the thrust audio is at its highest volume.

The explosion audio is enabled by AUD3. The volume of this signal is also determined by the state of AUD0 thru AUD2.

The 3 KHz audio and 6 KHz audio are enabled by AUD4 and AUD5 respectively. The 3 KHz signal is used as an audio warning of low fuel and indicator of proper ROM and RAM operation during Self-Test. The 6 KHz signal is used as the coin door SLAM audio and during Self-Test to indicate proper operation of control panel and coin door switch inputs and improper operation of ROM and RAM.



PART OF REGULATOR/AUDIO PCB



NOTE:
AUDIO AMPLIFIER IS PART OF REGULATOR/AUDIO PCB AND IS REPEATED ON SHEET 1, SIDE A.

The video output circuit consists of three individual circuits; X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits consists of a digital-to-analog (DAC) converter, current-to-voltage converter, sample and hold, sample and hold control, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (B11 and D11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the X axis, the number is 0 to 1,023, where 0 is at the far left of the monitor screen, 512 at the center, and 1,023 is at the far right. For the Y axis, the number is from 0 to 768, where 0 is at the bottom of the monitor screen, 384 is the center, and 768 is the top.

The DACs convert these binary number inputs to current output. The DAC's current output is applied to the pin 6 inputs of current-to-voltage converters A12 and C12. The pin 5 inputs ensure that the null points (resting point on the monitor screen) of the pin 7 outputs are 512 for the X axis and 384 for the Y axis.

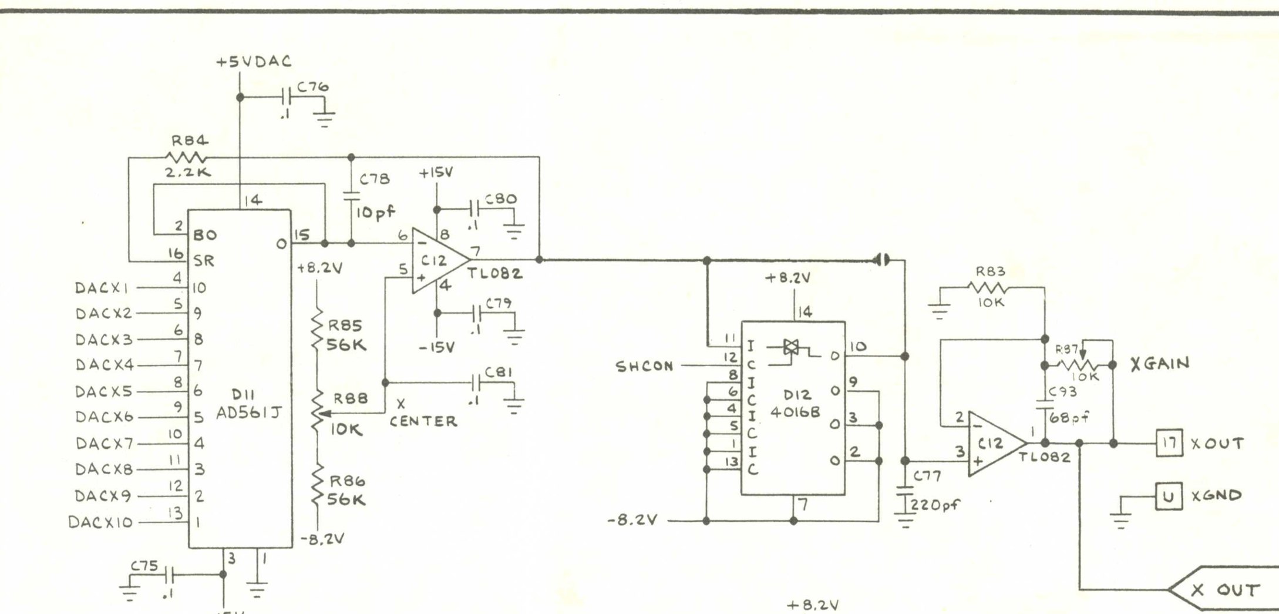
From the current-to-voltage converters, the signal is fed to the sample and hold circuits. Analog switches B12 and D12 pass the voltages to sample and hold capacitors C77 and C84. This is controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insure that the pin 7 outputs of voltage-to-current converters A12 and C12 have sufficiently stabilized before being applied to the sample and hold capacitors. The output swing of SHCON is -8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample and hold capacitor to the voltage value. The voltages are then applied to the second stages of A12 and C12 for an impedance matched output to the X and Y inputs of the monitor. Since the monitor doesn't have field adjustable X and Y gains, the gains are adjusted by variable resistors R87 and R93.

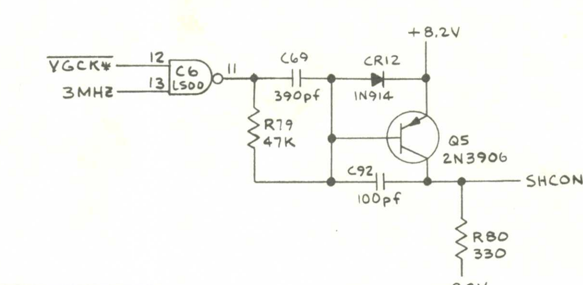
Z Output

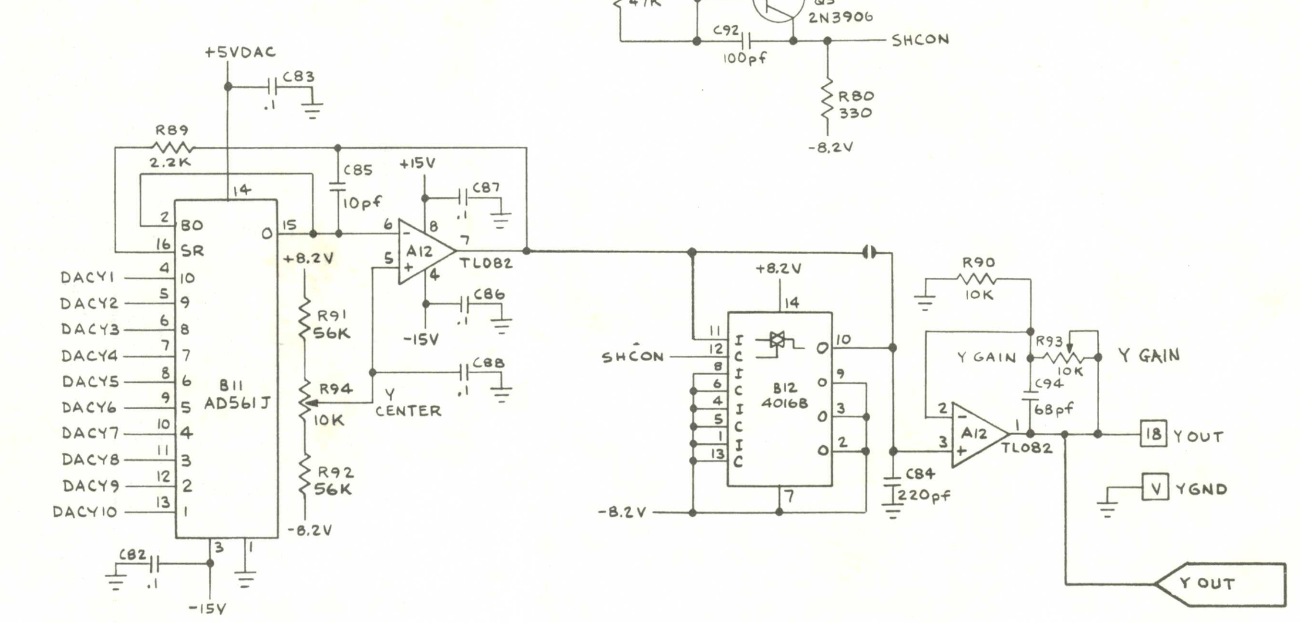
The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.

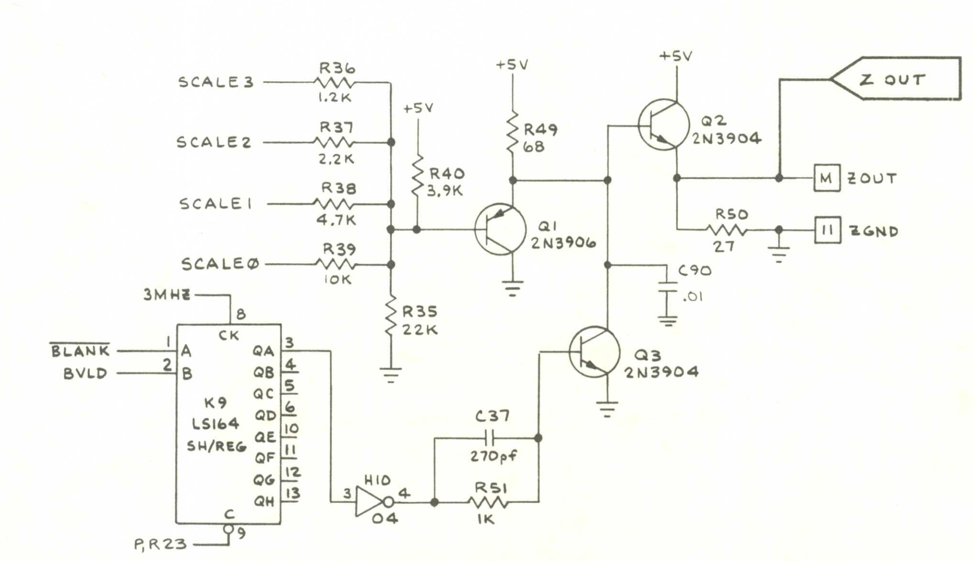
When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determines Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39,resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.









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