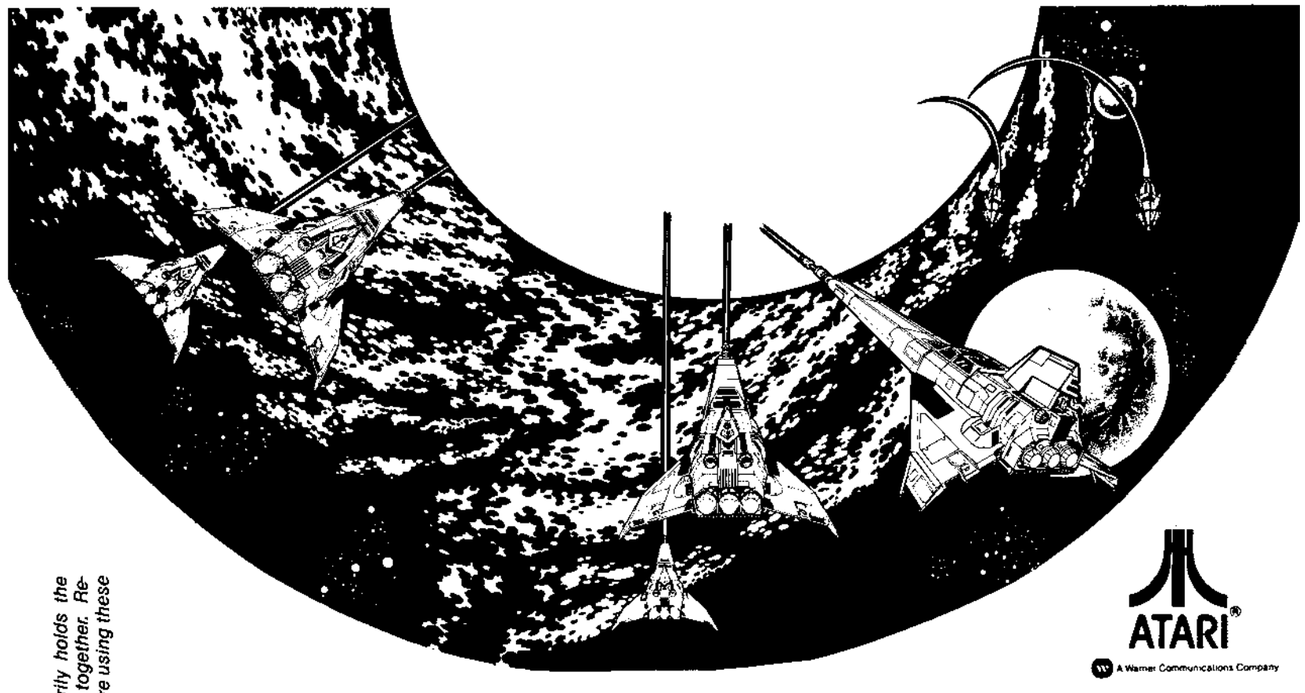
Table of Contents



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NOTE
This staple temporarily holds the schematic package together. Remove the staple before using these schematics.

Schematic Package Supplement to

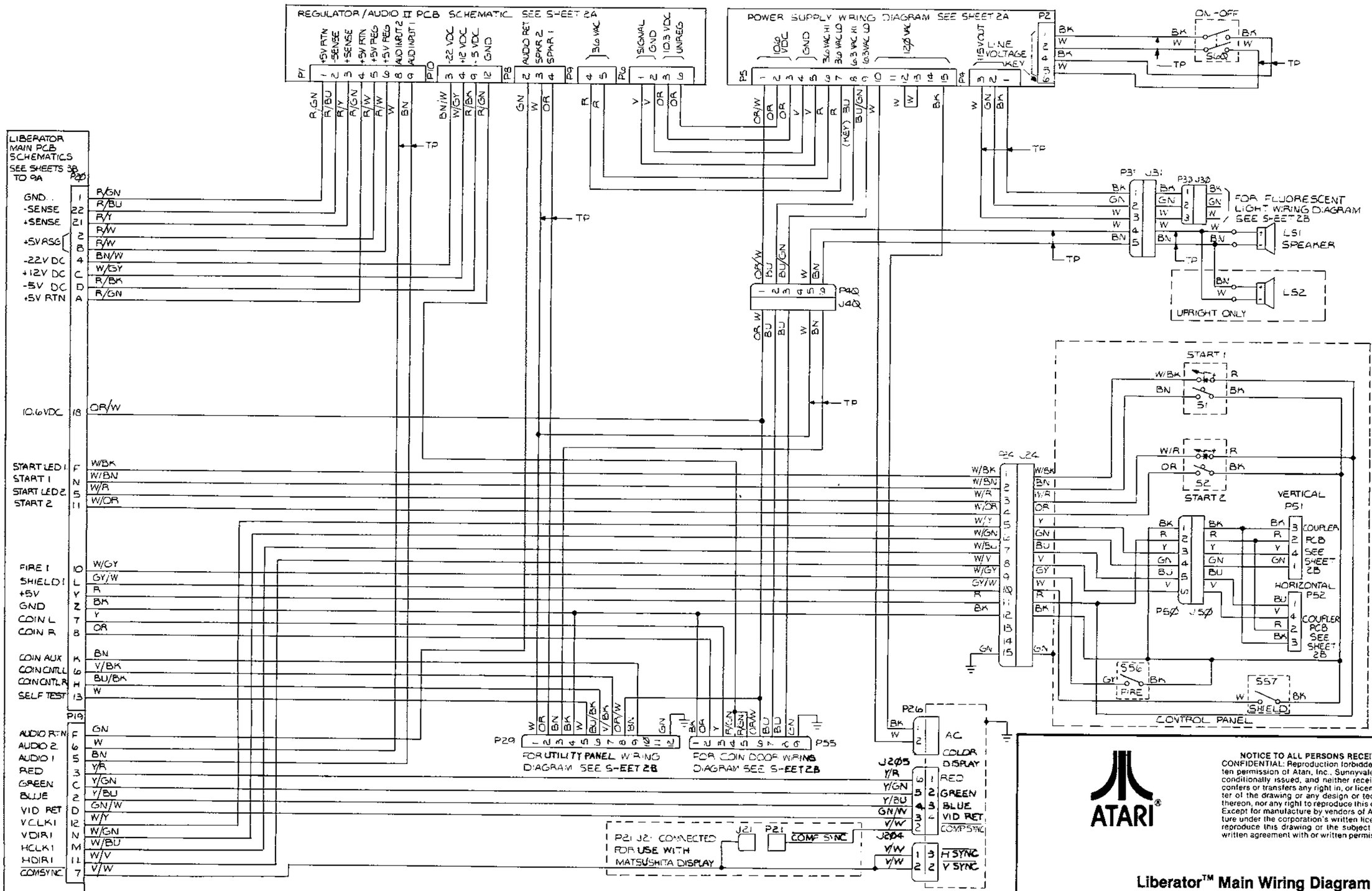
TM

LIBERATOR

Operation, Maintenance, and Service Manual

10L

SP-209 Sheet 1A
1st Printing



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Liberator™ Main Wiring Diagram

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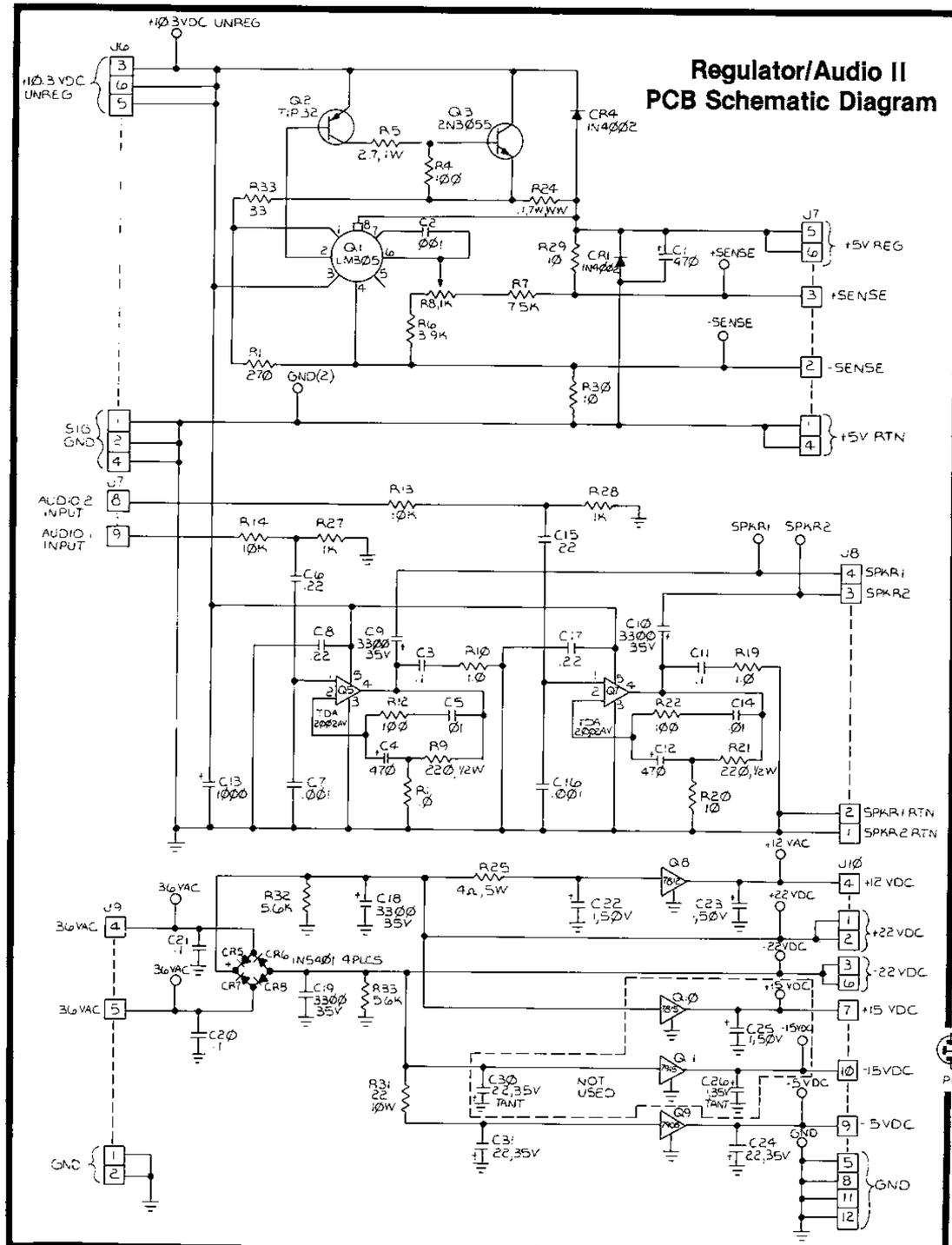
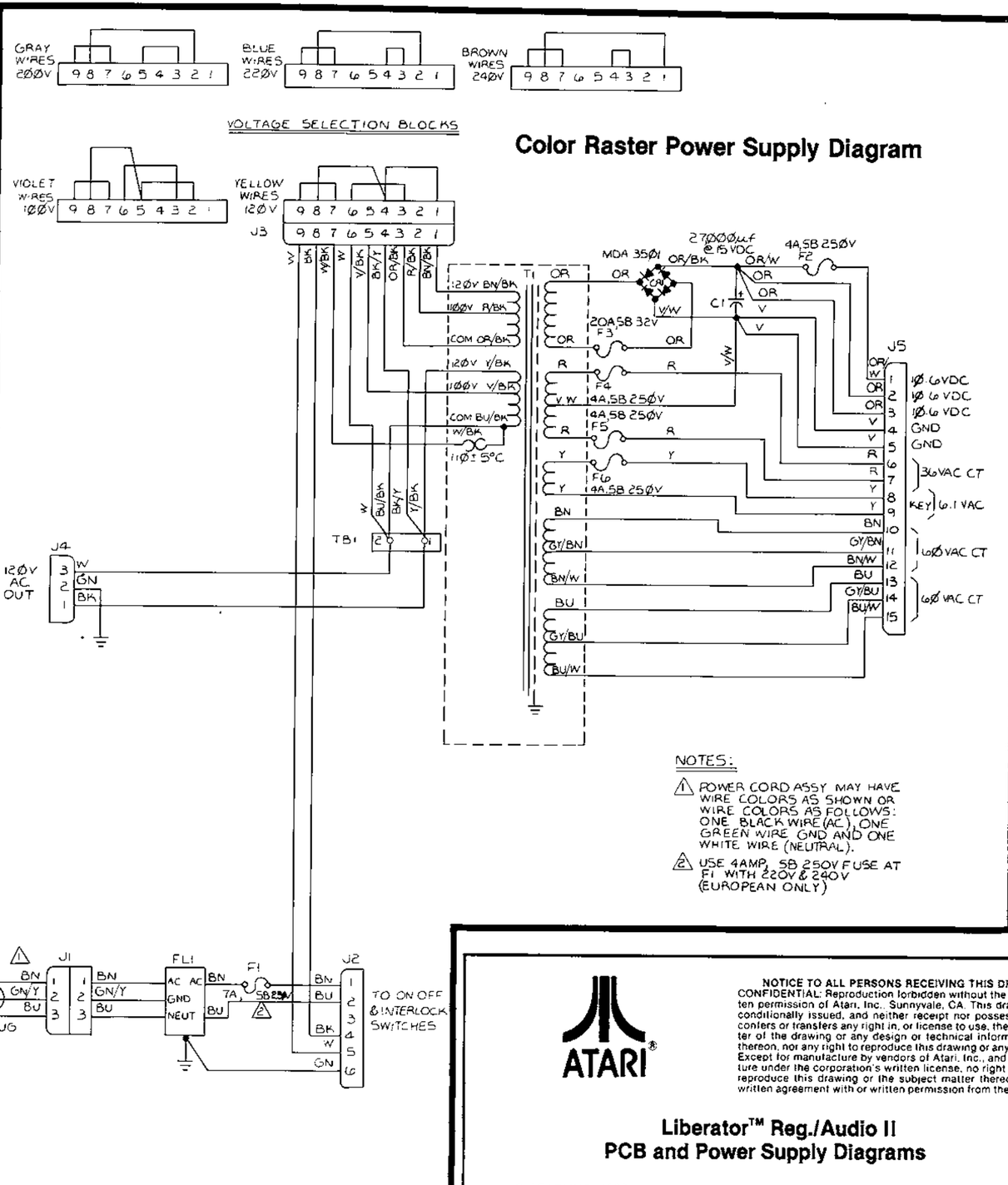
SP-209 Sheet 1B
1st Printing

Regulator/Audio II PCB Schematic Diagram



Color Raster Power Supply Diagram



NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE GND AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY)

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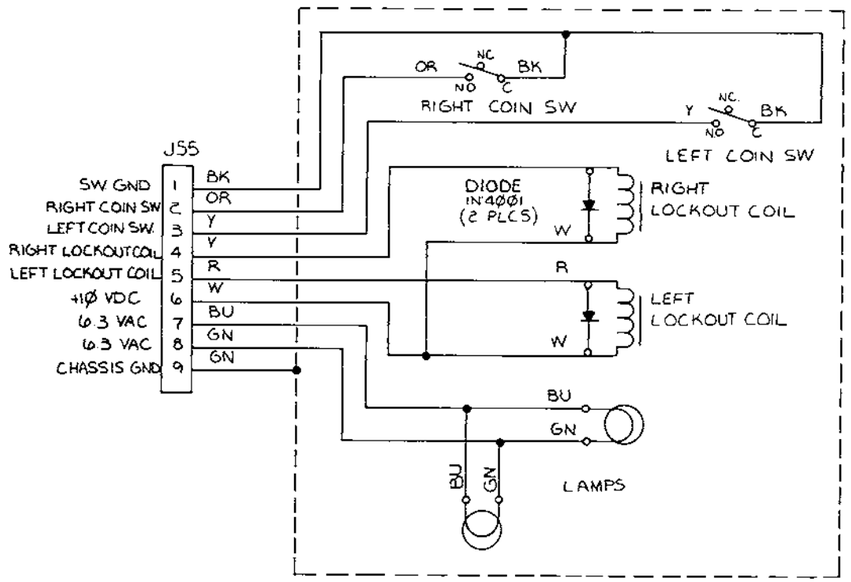
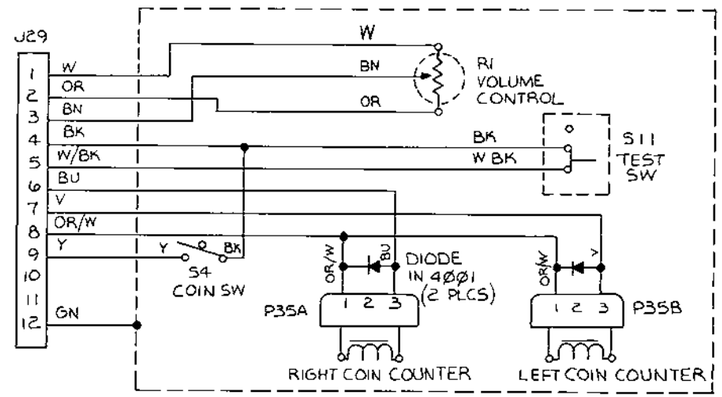
Liberator™ Reg./Audio II PCB and Power Supply Diagrams

SP-209 Sheet 2A
1st Printing

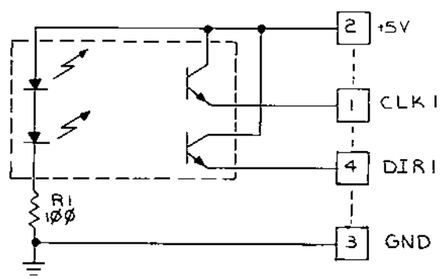
Coin-Door Wiring Diagram



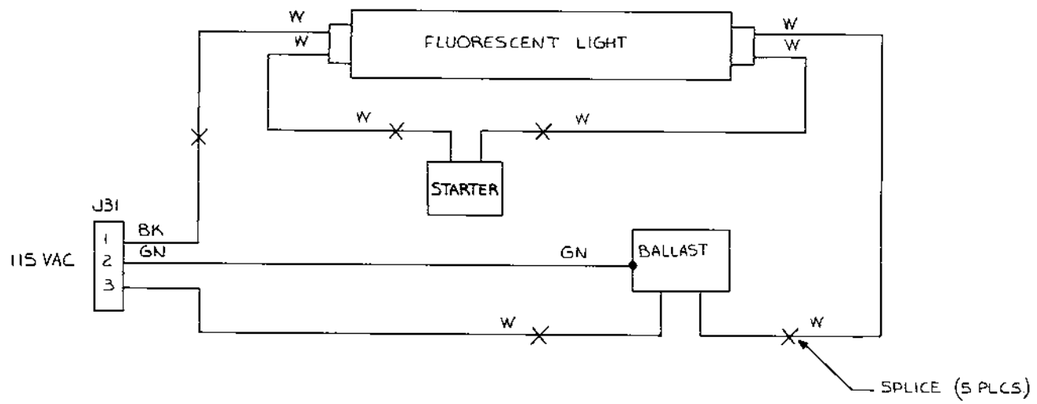
Utility Panel Wiring Diagram



Coupler PCB Schematic



Fluorescent Light Wiring Diagram



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Liberator™ Game Wiring Interfaces

SP-209 Sheet 2B
1st Printing

MEMORY MAP

HEXA-DECIMAL ADDRESS	ADDRESS BUS A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		D	D	D	D	D	D	D	D	XCOORD
0001	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		D	D	D	D	D	D	D	D	YCOORD
0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		D	D	D						BIT MODE DATA
0003-033F 0340-303F 3D40-3FFF	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	WORKING RAM SCREEN RAM WORKING RAM
4000	0	1	0	0	0												R	D	D	D	D	D	D	D	D	EARD
5000	0	1	0	1	0											0	R								D	COIN AUX (CTRLD SET LOW)
																								D		COIN LEFT (CTRLD SET LOW)
																							D			COIN RIGHT (CTRLD SET LOW)
																						D				SLAM (CTRLD SET LOW)
																					D					SPARE (CTRLD SET LOW)
																				D						SPARE (CTRLD SET LOW)
																			D							COCKTAIL (CTRLD SET LOW)
																		D								SELF-TEST (CTRLD SET LOW)
																						D	D	D	D	HDIR (CTRLD SET HIGH)
																		D	D	D	D					VDIR (CTRLD SET HIGH)
5001	0	1	0	1	0											1	R								D	SHIELD 2
																								D		SHIELD 1
																							D			FIRE 2
																						D				FIRE 1
																					D					SPARE
																				D						START 2
																			D							START 1
																		D								VBLANK
6000-6000F	0	1	1	0	0	0	0							A	A	A	A	W					D	D	D	D	BASRAM
6200-621F	0	1	1	0	0	0	1							A	A	A	A	W	D	D	D	D	D	D	D	D	COLORAM
6400	0	1	1	0	0	1	0											W									INTACK
6600	0	1	1	0	0	1	1											W					D	D	D	D	EARCON
6800	0	1	1	0	1	0	0											W	D	D	D	D	D	D	D	D	STARTLG
6A00	0	1	1	0	1	0	1											W									WDOG
6C00	0	1	1	0	1	1	0									0	0	W				D					START LED 1
6C01																0	0	W				D					START LED 2
6C02																0	1	W				D					TBSWP
6C03																0	1	W				D					SPARE
6C04																1	0	W				D					CTRLD
6C05																1	0	W				D					COINCNTRR
6C06																1	1	W				D					COINCNTRL
6C07																1	1	W				D					PLANET
6E00-6E3F	0	1	1	0	1	1	1							A	A	A	A	W	D	D	D	D	D	D	D	D	EARWR
7000-701F	0	1	1	1	0									A	A	A	A		D	D	D	D	D	D	D	D	IOS2
7800-781F	0	1	1	1	1									A	A	A	A		D	D	D	D	D	D	D	D	IOS1
8000-EFFF	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	ROM

Schematic Reference Designators and Symbols

Logic symbols depict the logic function performed by that particular device and may differ from the manufacturer's data.

REFERENCE DESIGNATORS:

C	Capacitor
CR	Diode, signal or rectifier
F	Fuse
J	Connector
L	Inductor, fixed or variable
LS	Speaker
P	Connector
Q	Transistor or silicon-controlled rectifier
R	Resistor, fixed or variable
S	Switch
T	Transformer
TP	Twisted wire pair
VR	Voltage regulator
Y	Crystal

WIRE COLORS:

R	Red
GN	Green
Y	Yellow
W	White
BU	Blue
BN	Brown
BK	Black
OR	Orange
V	Violet
GY	Gray

Electrical components shown on the schematic diagrams are in the following units unless otherwise noted:

Capacitors = microfarads (μf)
Resistors = ohms (Ω)
Inductors = microhenrys (μh)

SYMBOLS:

Ground

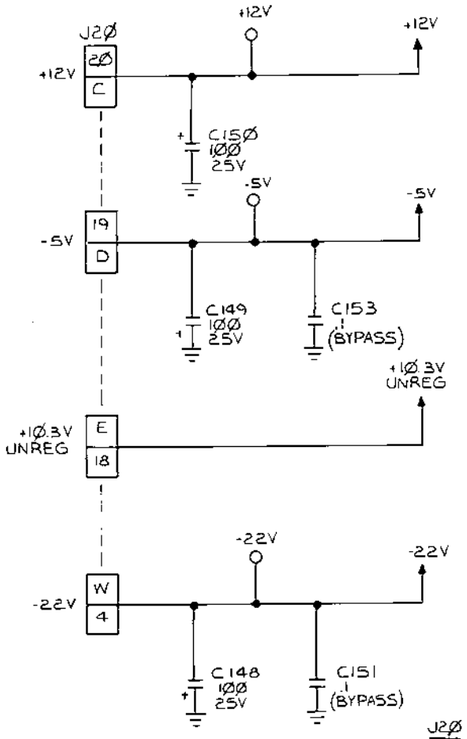
Test Point

PCB edge connector pad

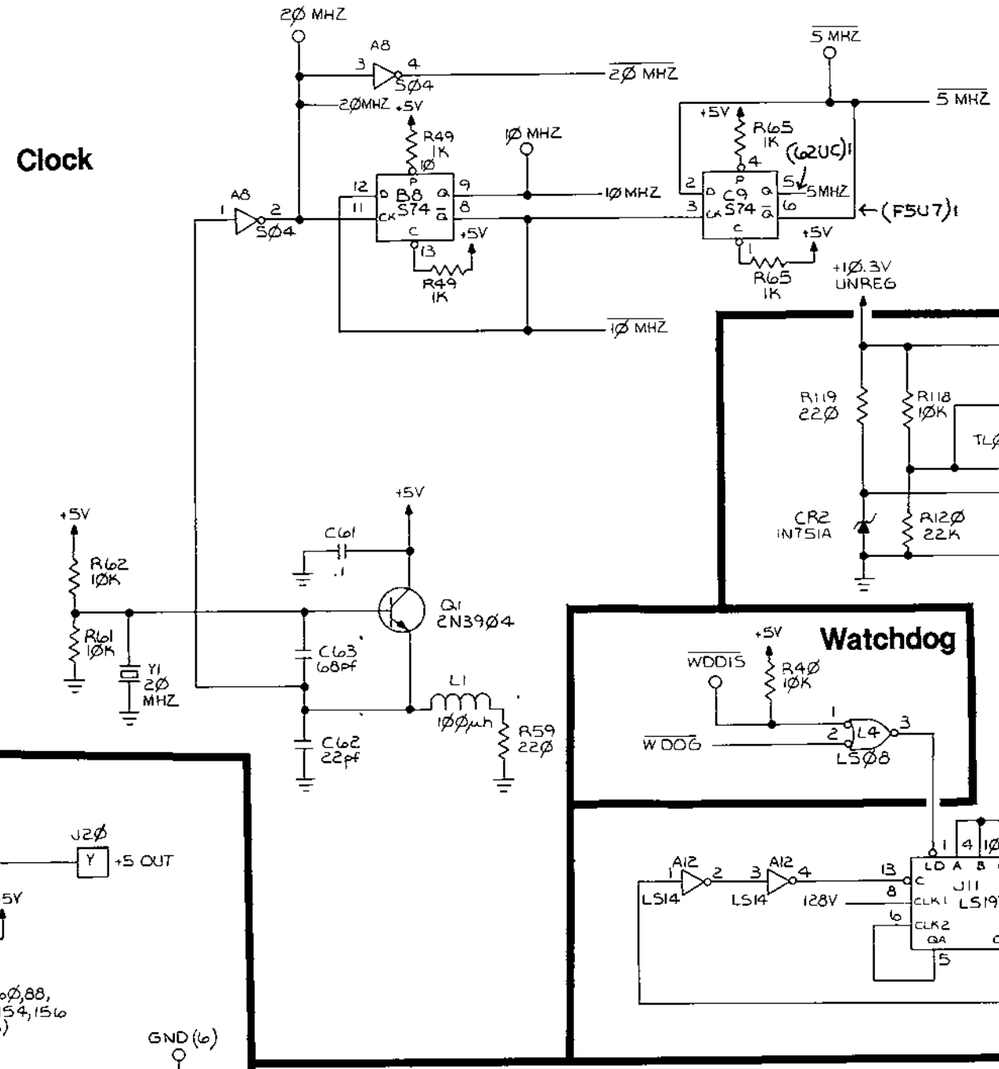
PCB test connector pad

Liberator™ Memory Map and Schematic Notes

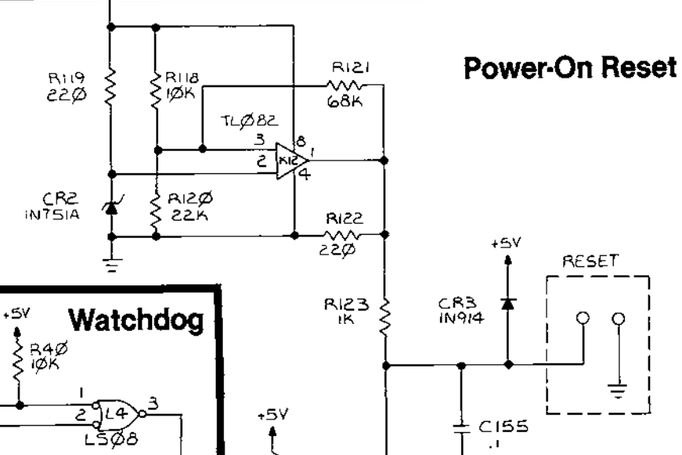
Power Input



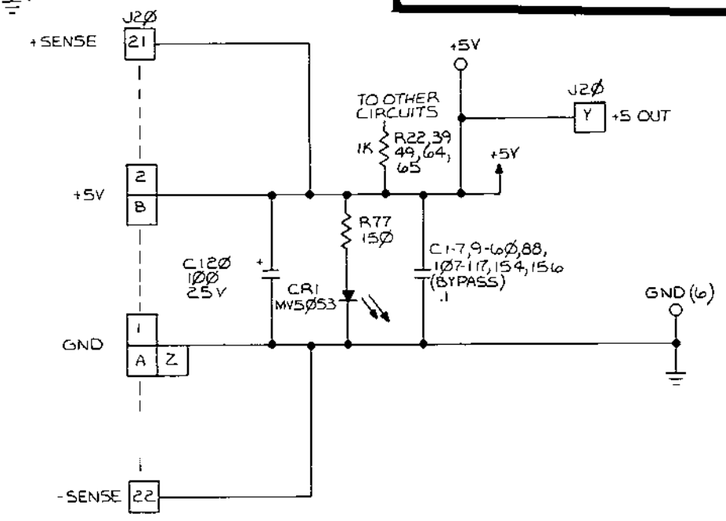
Clock



Power-On Reset



Watchdog



NOTE

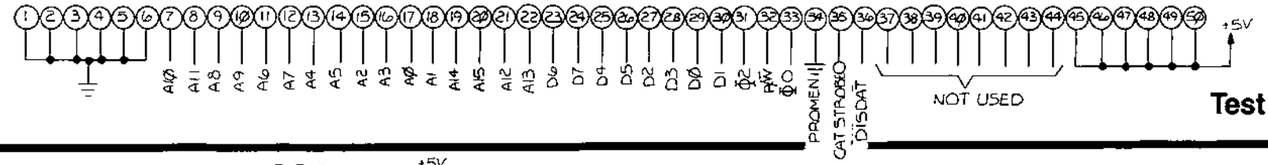
To avoid faulty readings while testing signatures, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

Liberator™ PCB Schematic Diagram

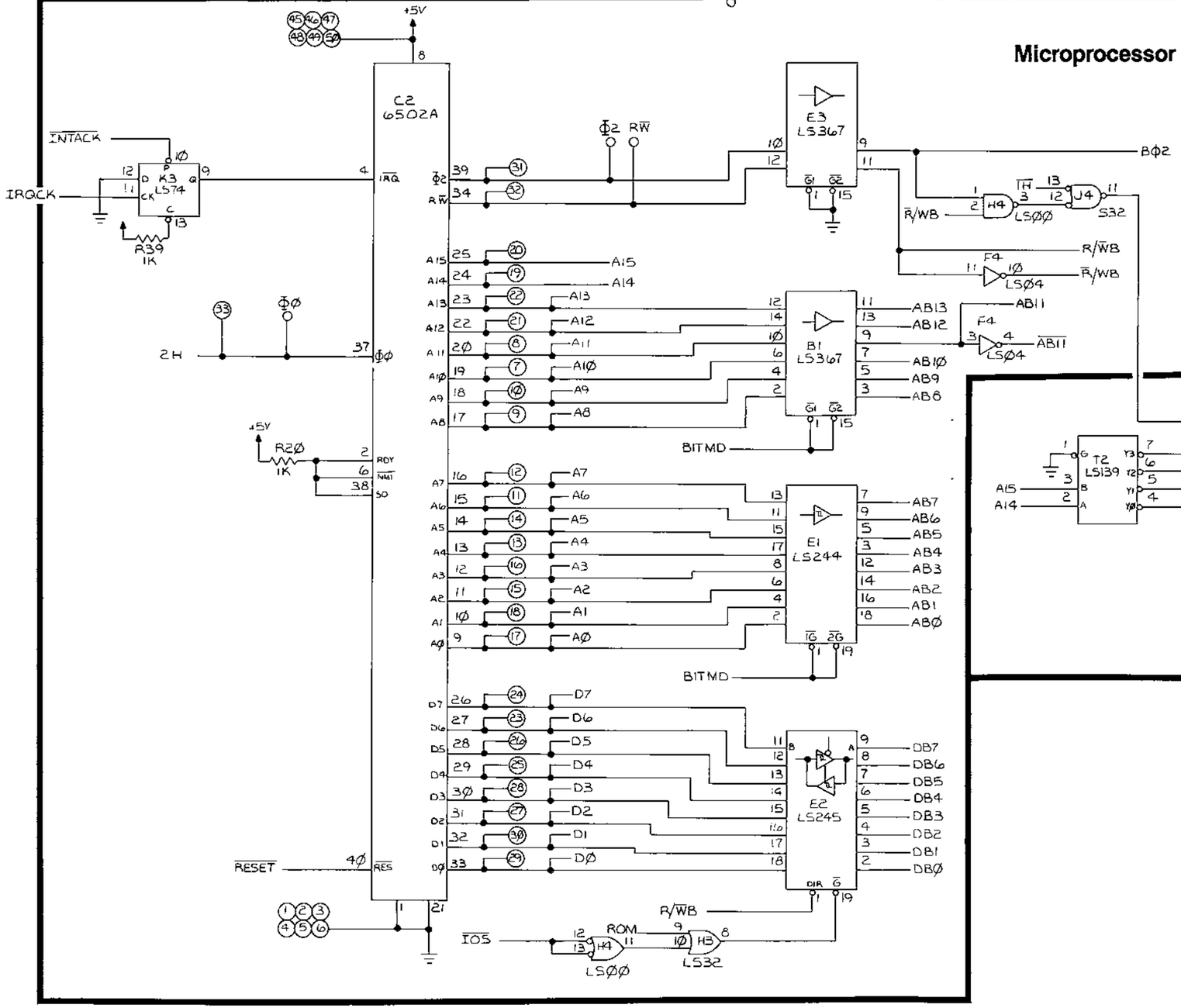
SP-209 Sheet 3B

1st Printing

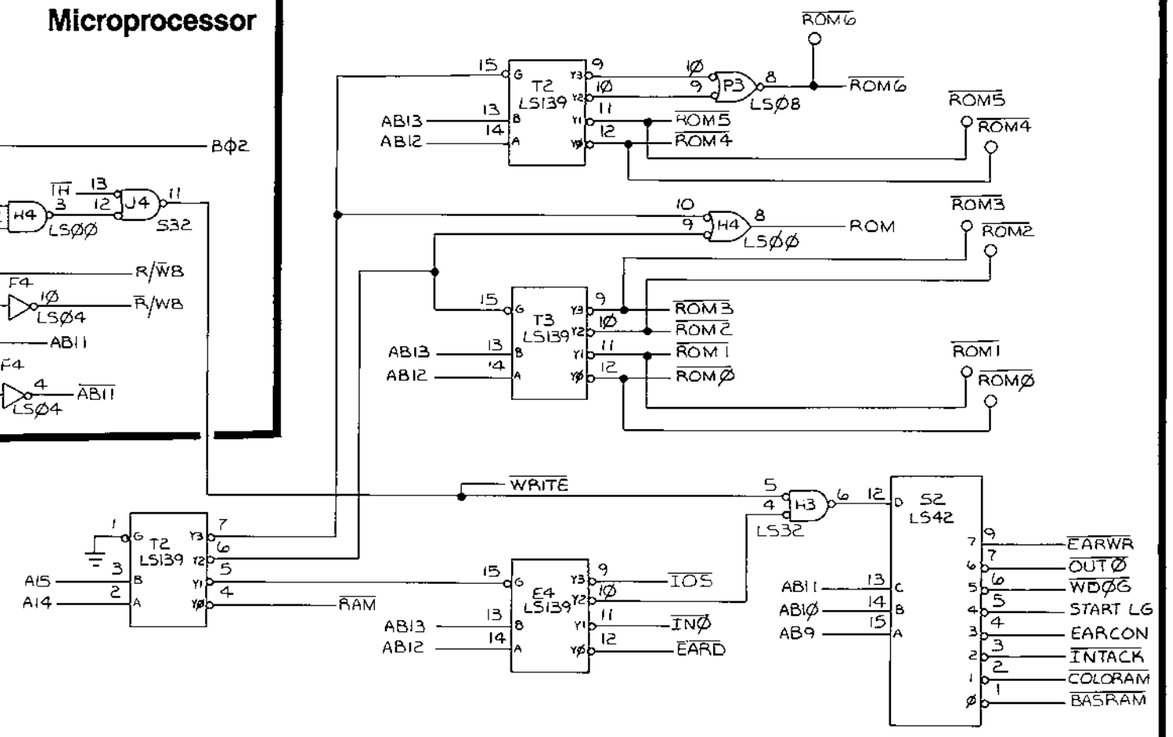
Test Connector



Microprocessor



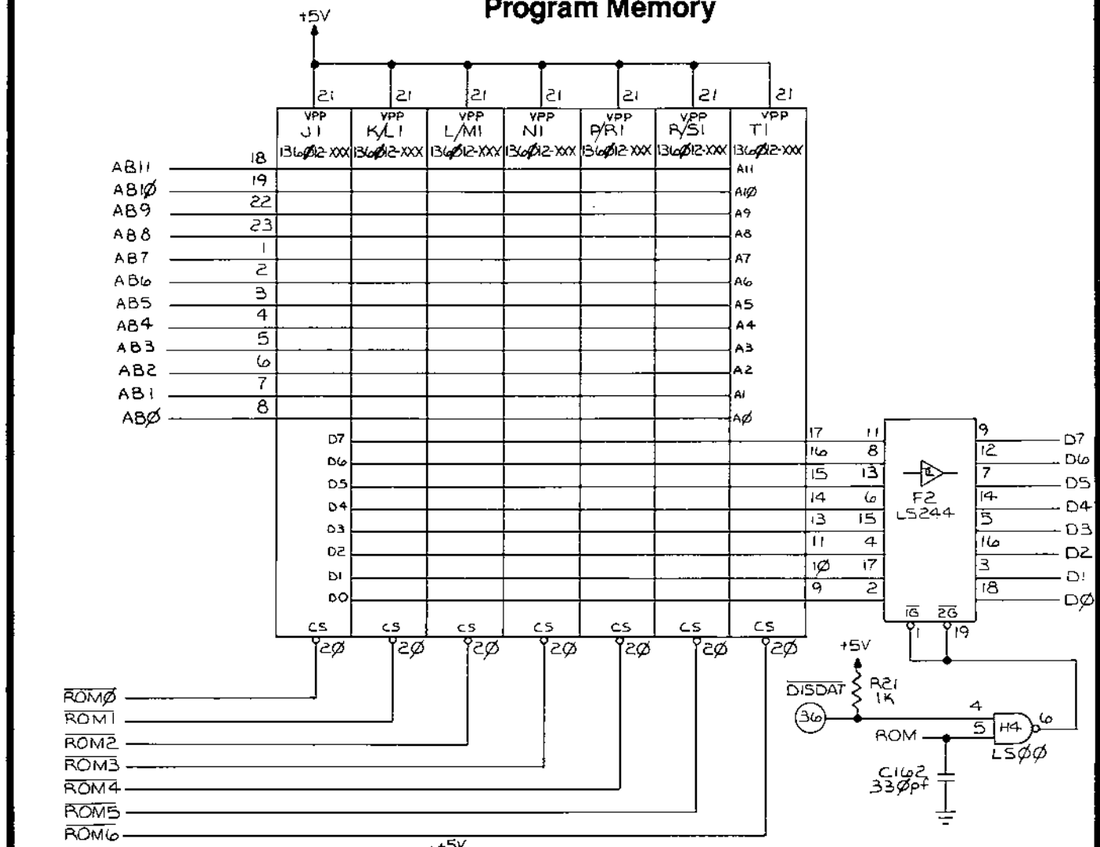
Address Decoders



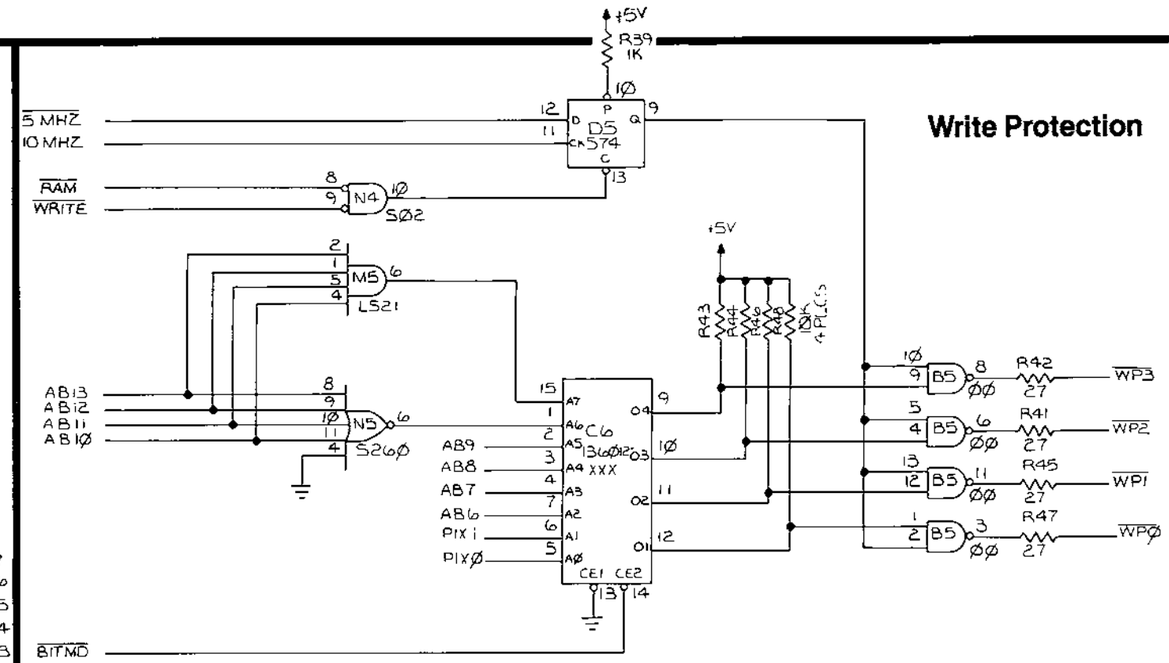
Liberator™ PCB Schematic Diagram

SP-209 Sheet 4A
1st Printing

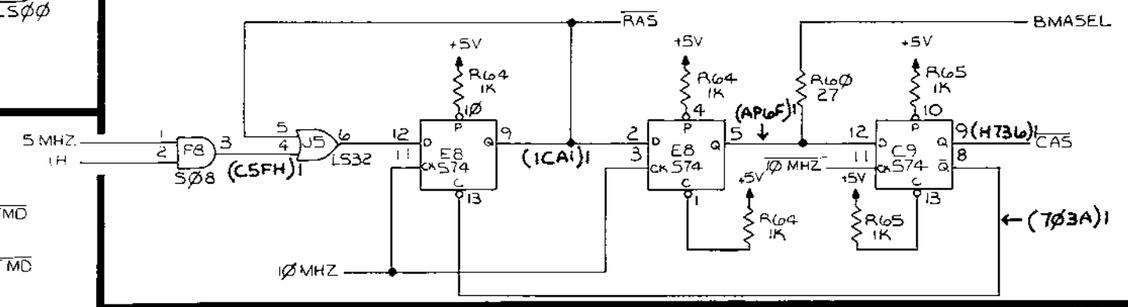
Program Memory



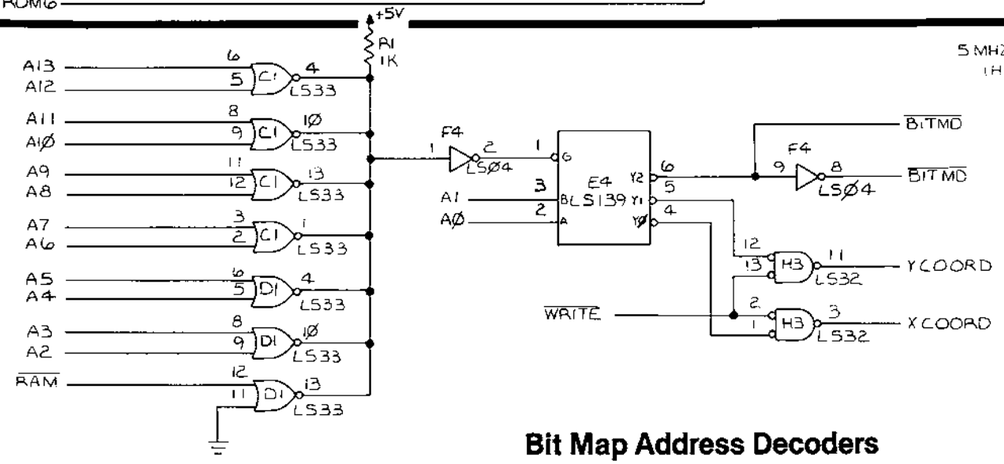
Write Protection



Refresh



Bit Map Address Decoders



NOTE

To avoid faulty readings while testing signatures, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

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Liberator™ PCB Schematic Diagram

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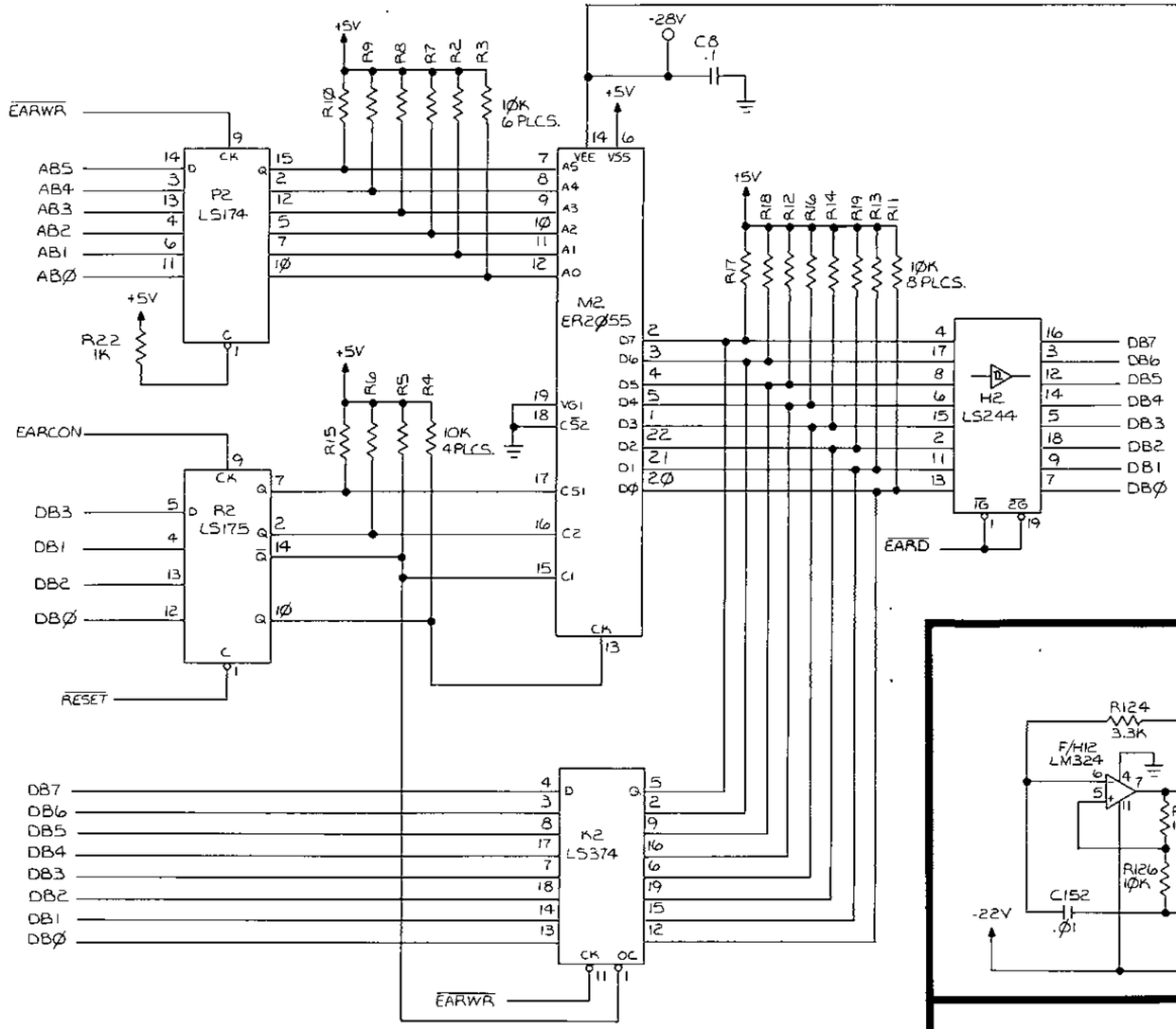
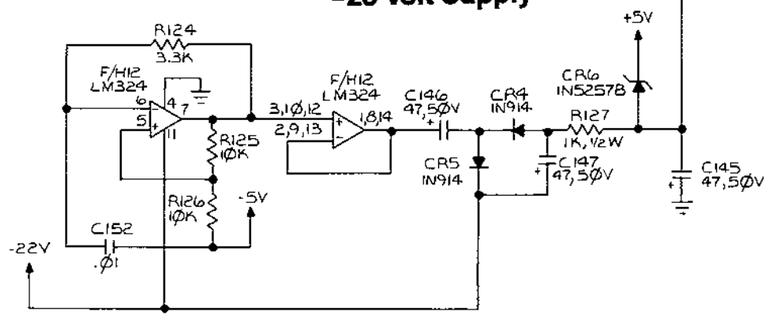
1st Printing

EAROM



-28 Volt Supply



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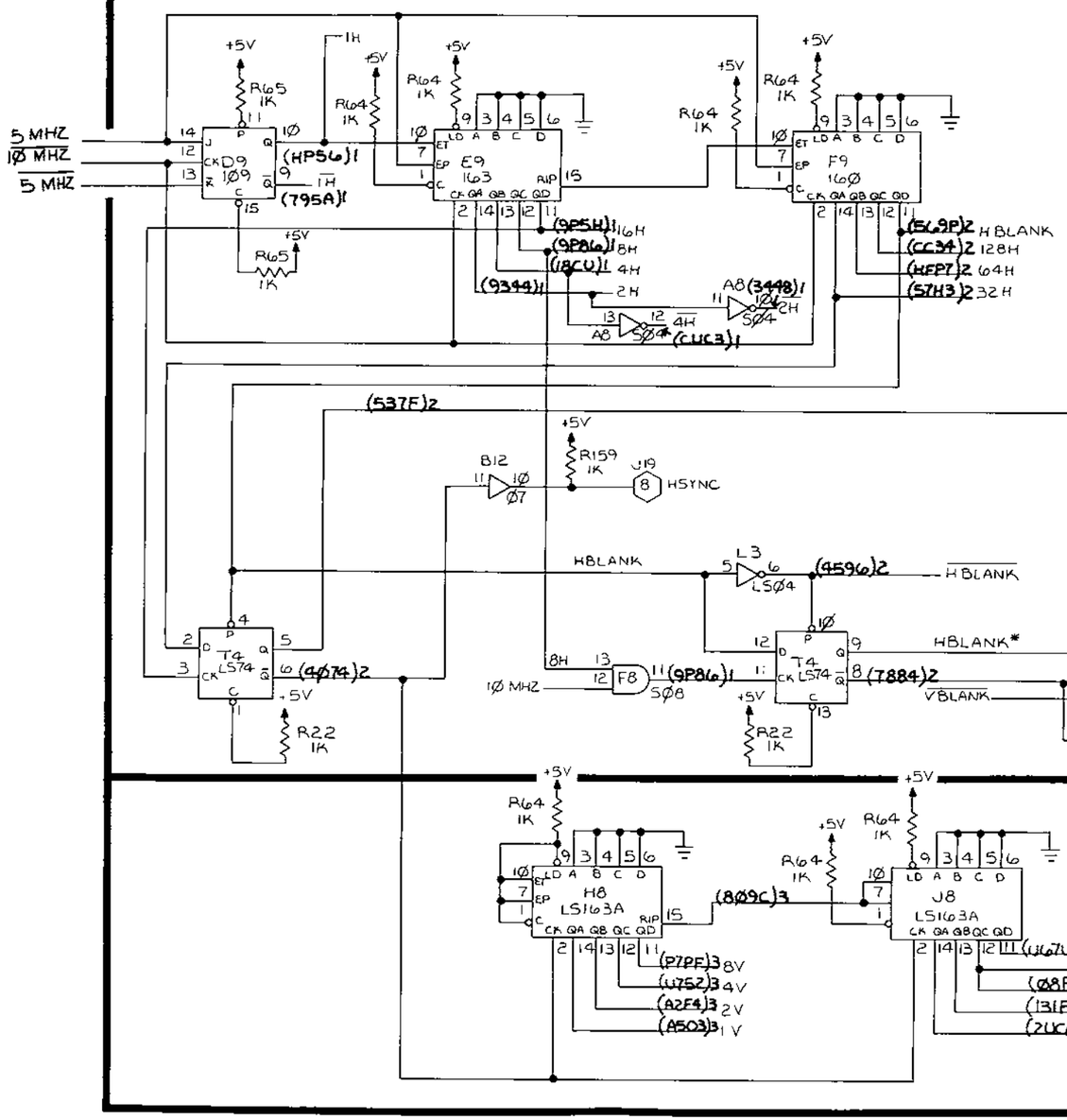
Liberator™ PCB Schematic Diagram

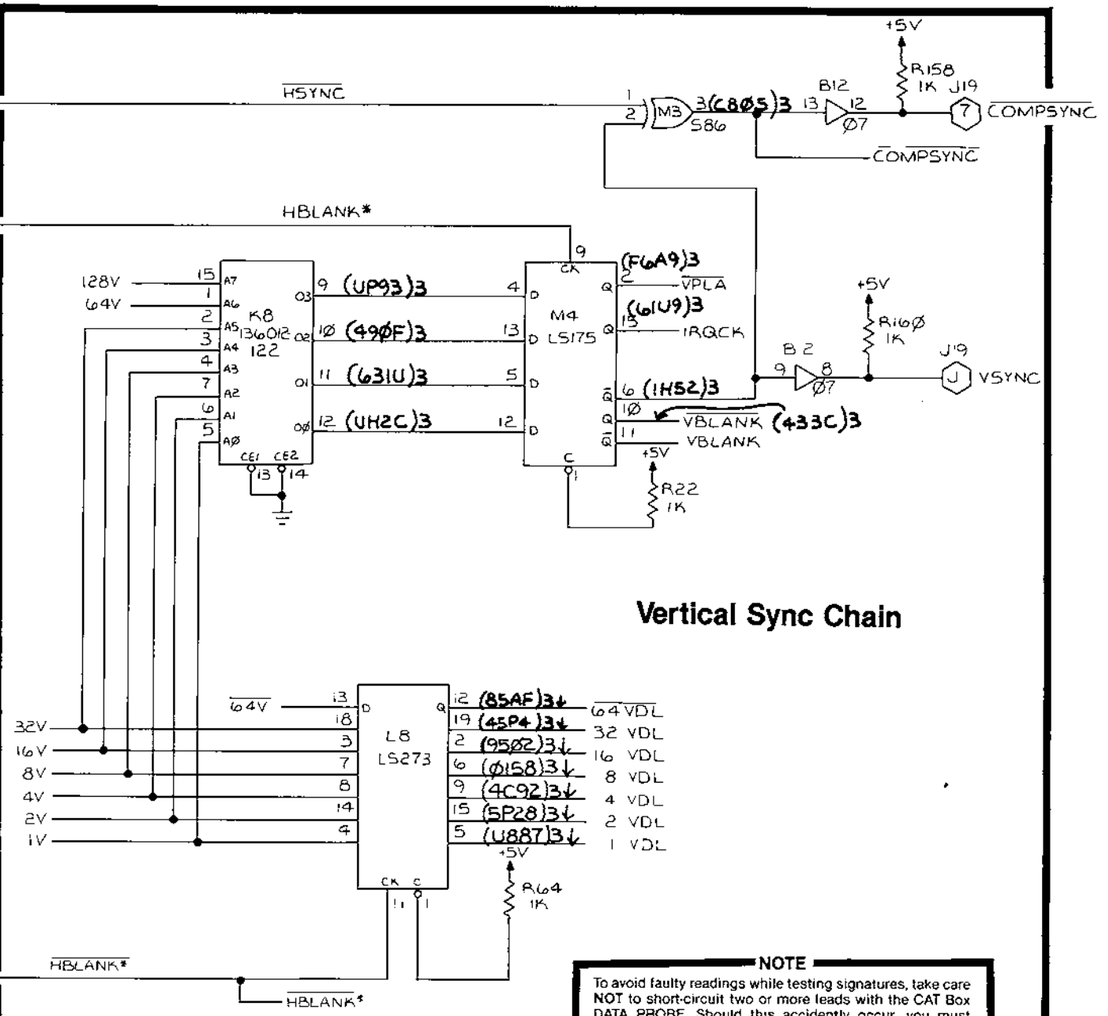
A Warner Communications Company

SP-209 Sheet 5A
1st Printing

Horizontal Sync Chain



Vertical Sync Chain



NOTE

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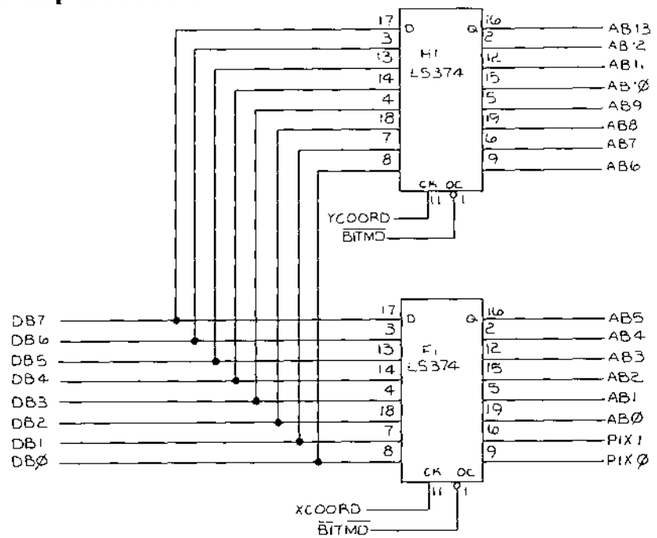
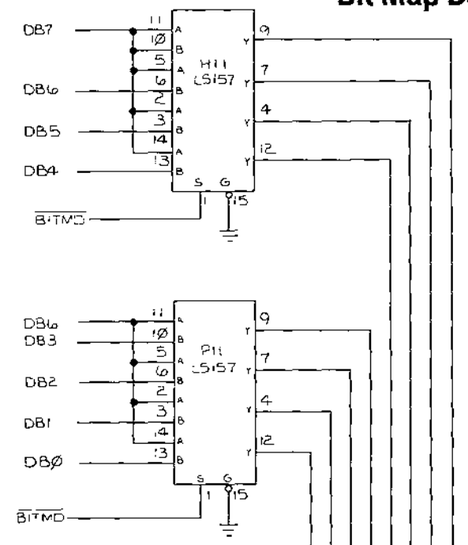
Liberator™ PCB Schematic Diagram

SP-209 Sheet 5B
1st Printing

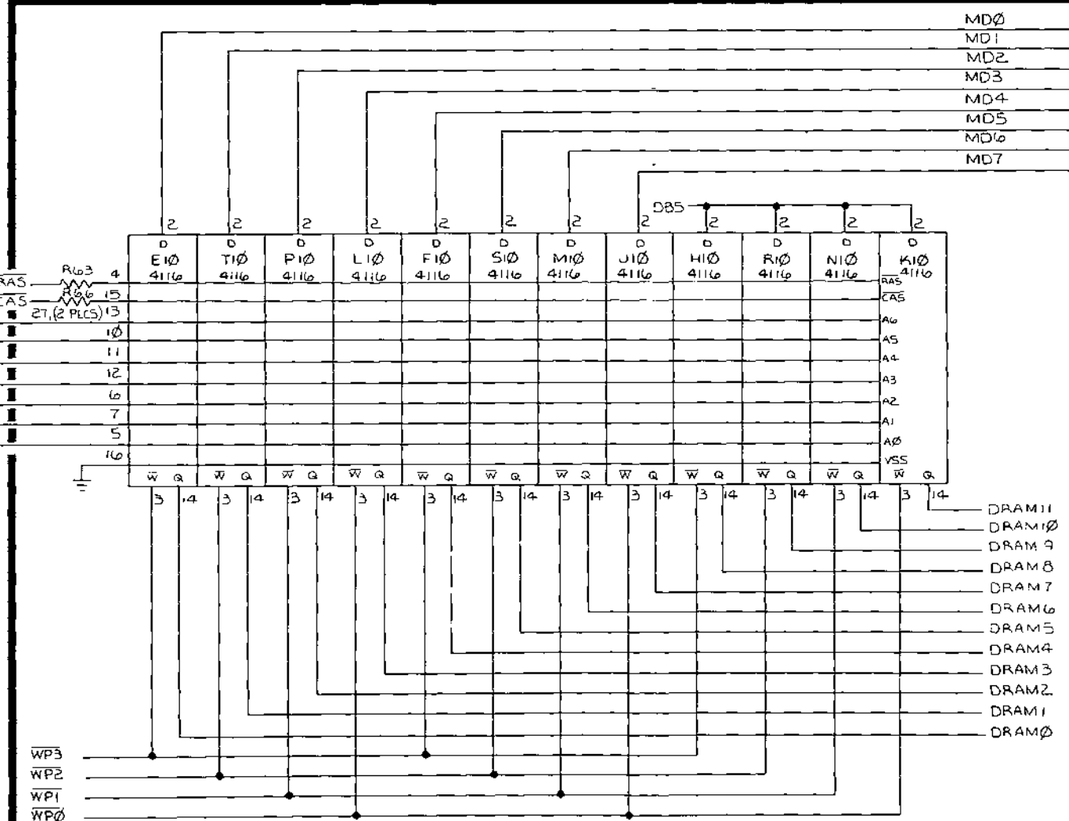
Bit Map Decoders



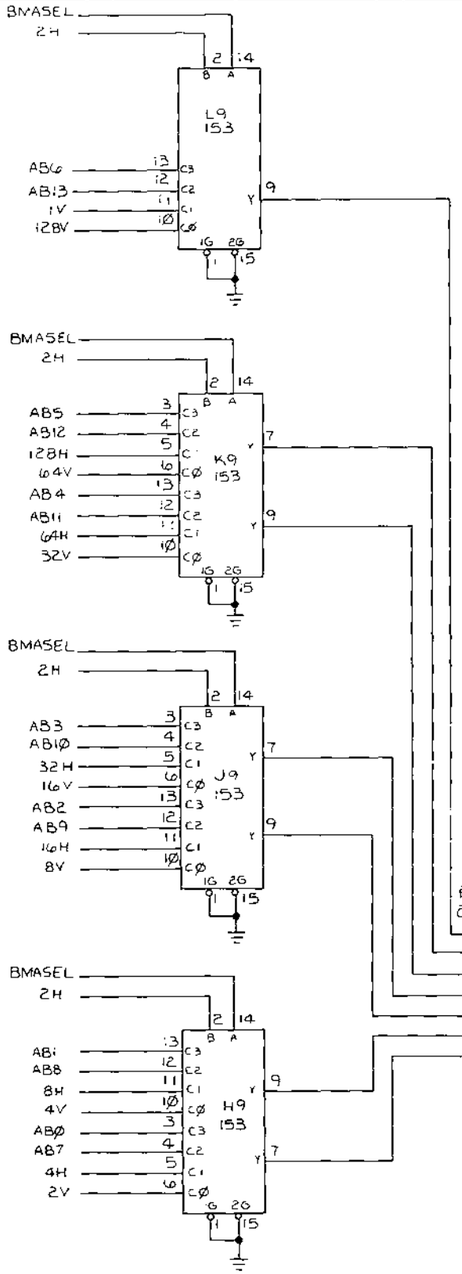
Bit Map Data Multiplexers



Bit Map Memory



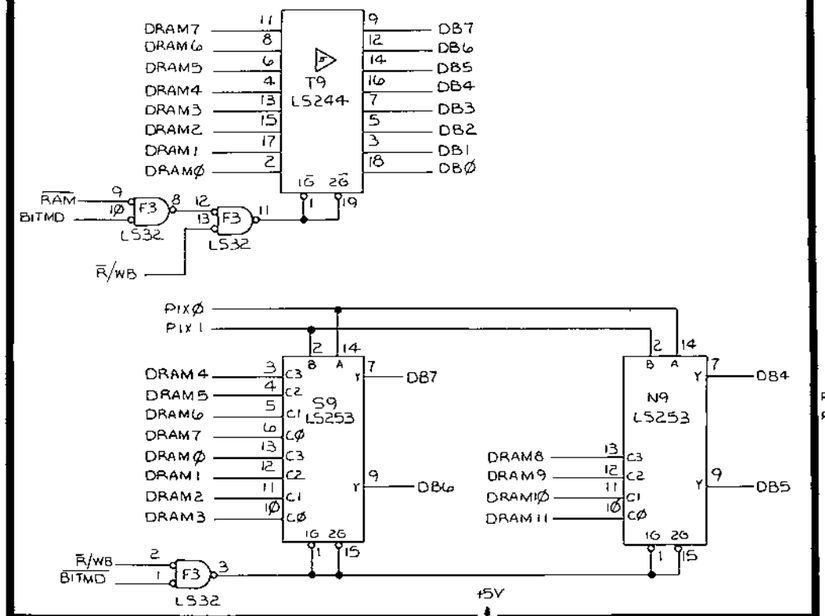
Bit Map Address Multiplexers



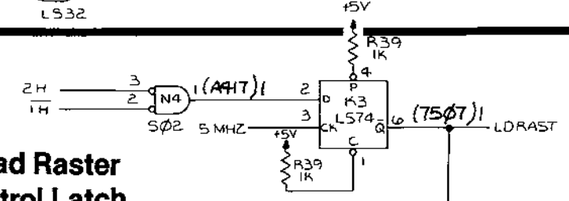
Liberator™ PCB Schematic Diagram

SP-209 Sheet 6A
1st Printing

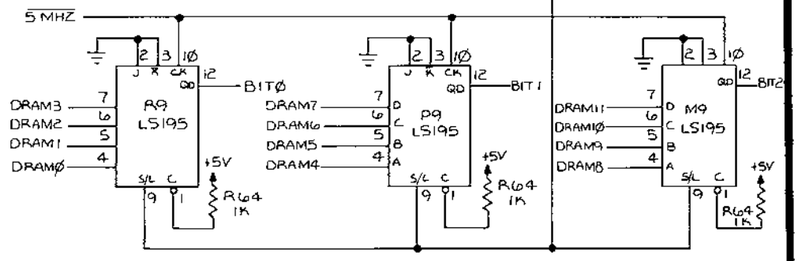
Bit Map Data Buffers



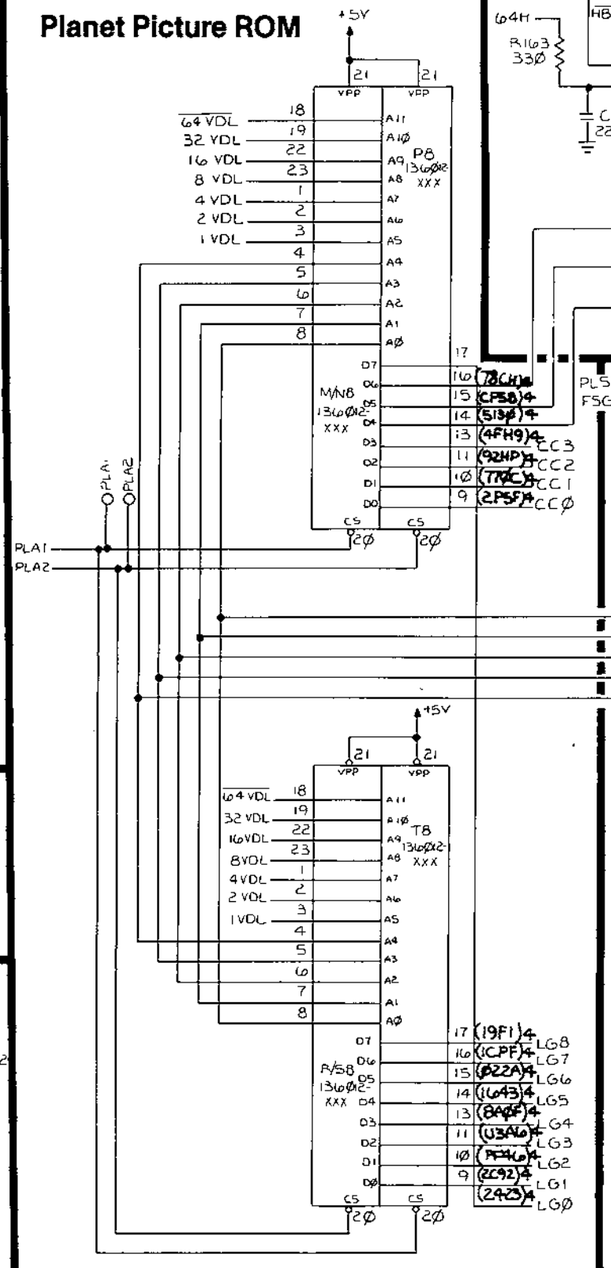
Load Raster Control Latch



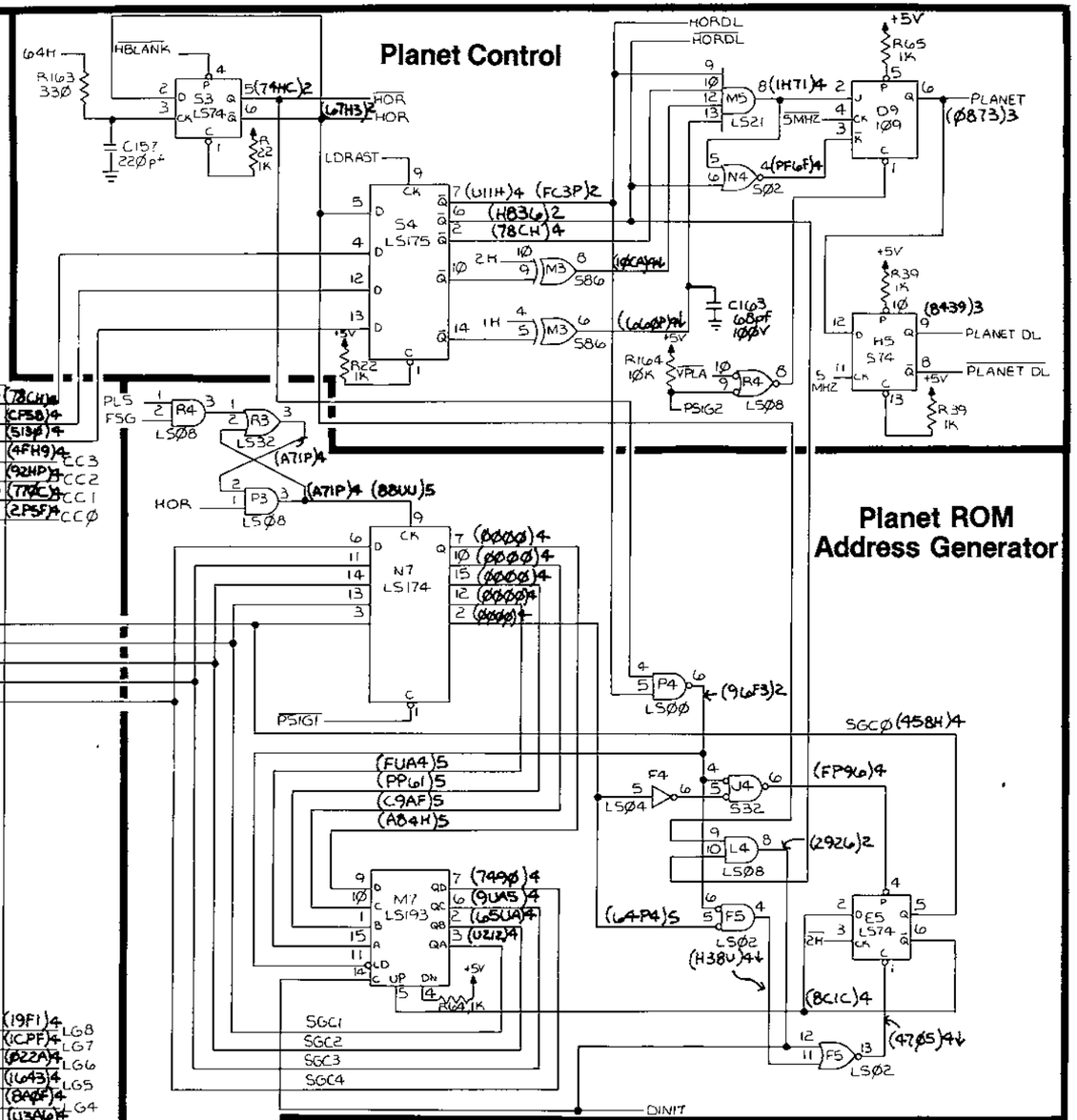
Bit Map Shift Registers



Planet Picture ROM



Planet Control



Planet ROM Address Generator

NOTE

To avoid faulty readings while testing signatures, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

Liberator™ PCB Schematic Diagram

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1st Printing

Longitude Scaling

Multiplier

Multiply Clock

Latitude Scaling

NOTE

To avoid faulty readings while testing signatures, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

Liberator™ PCB Schematic Diagram

Line Buffer Address Controller

Base RAM

Line Buffer

Valid Segment Detector

NOTE

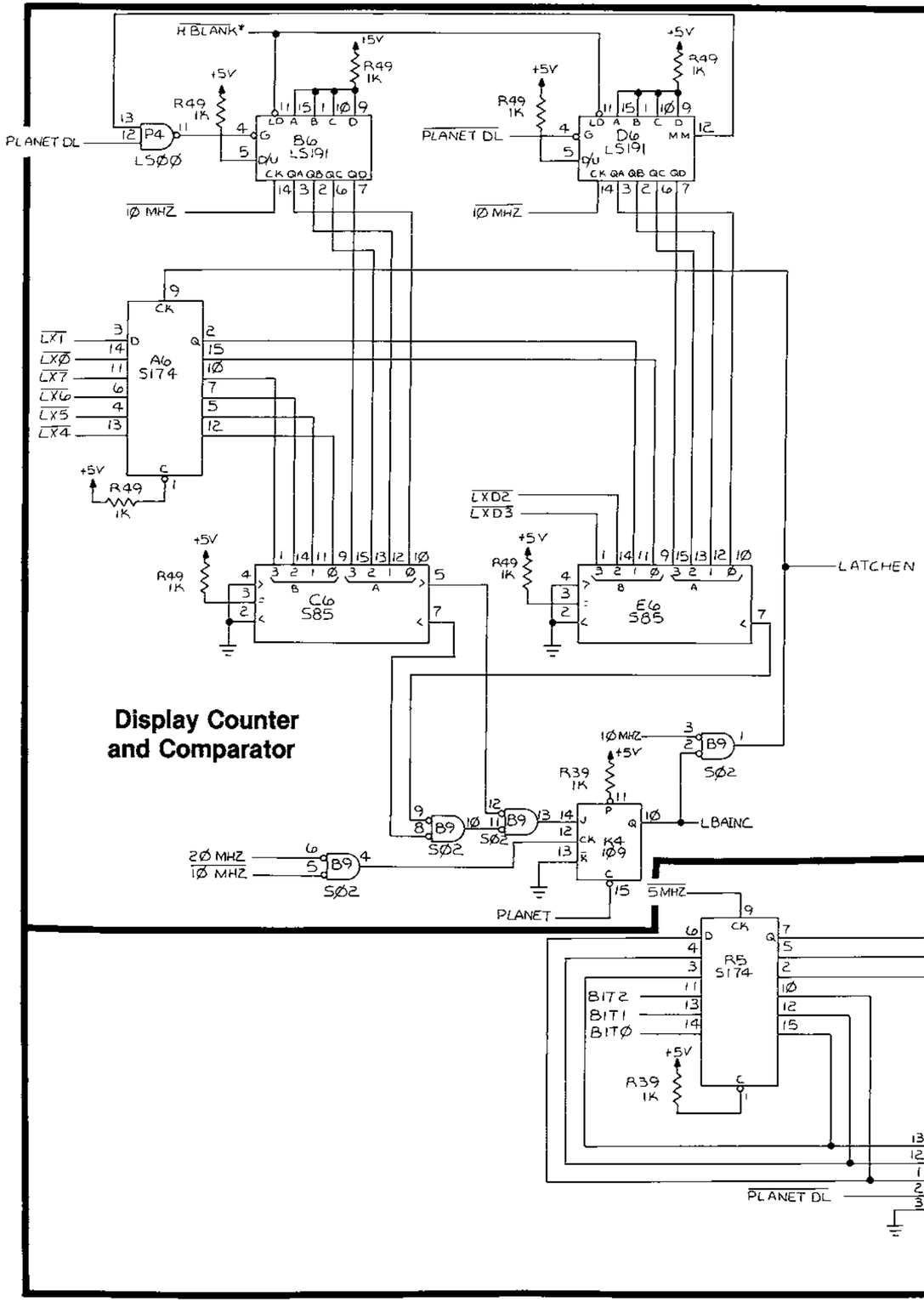
To avoid faulty readings while testing signatures, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

Liberator™ PCB Schematic Diagram

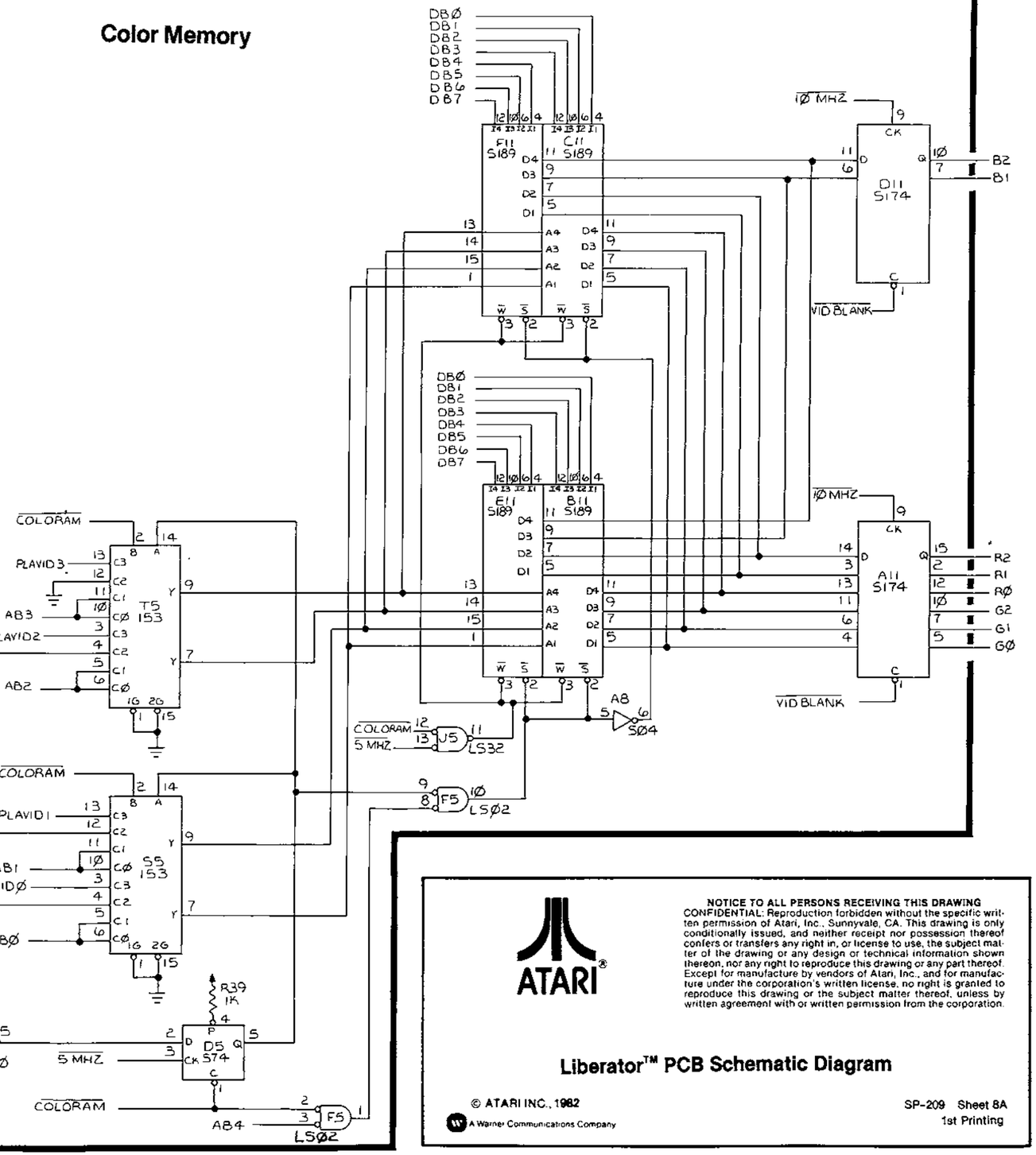
SP-209 Sheet 7B

1st Printing

Display Counter and Comparator



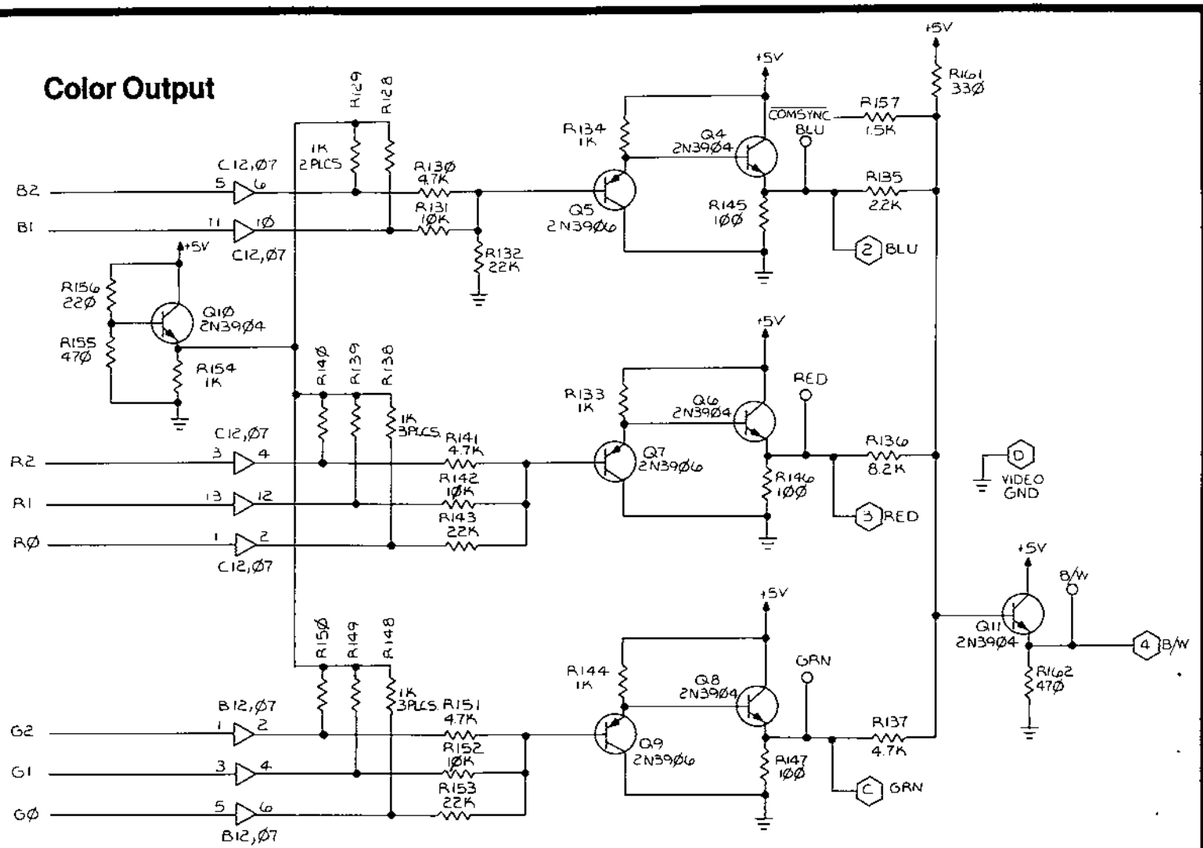
Color Memory



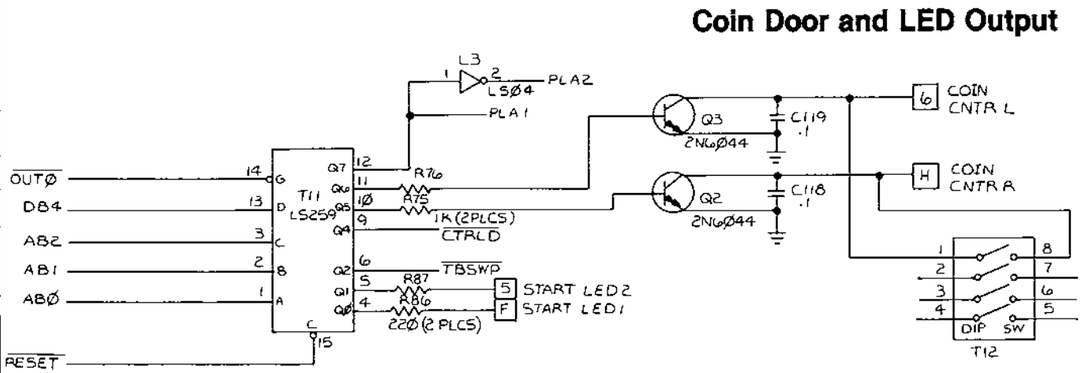
Liberator™ PCB Schematic Diagram

SP-209 Sheet 8A
1st Printing

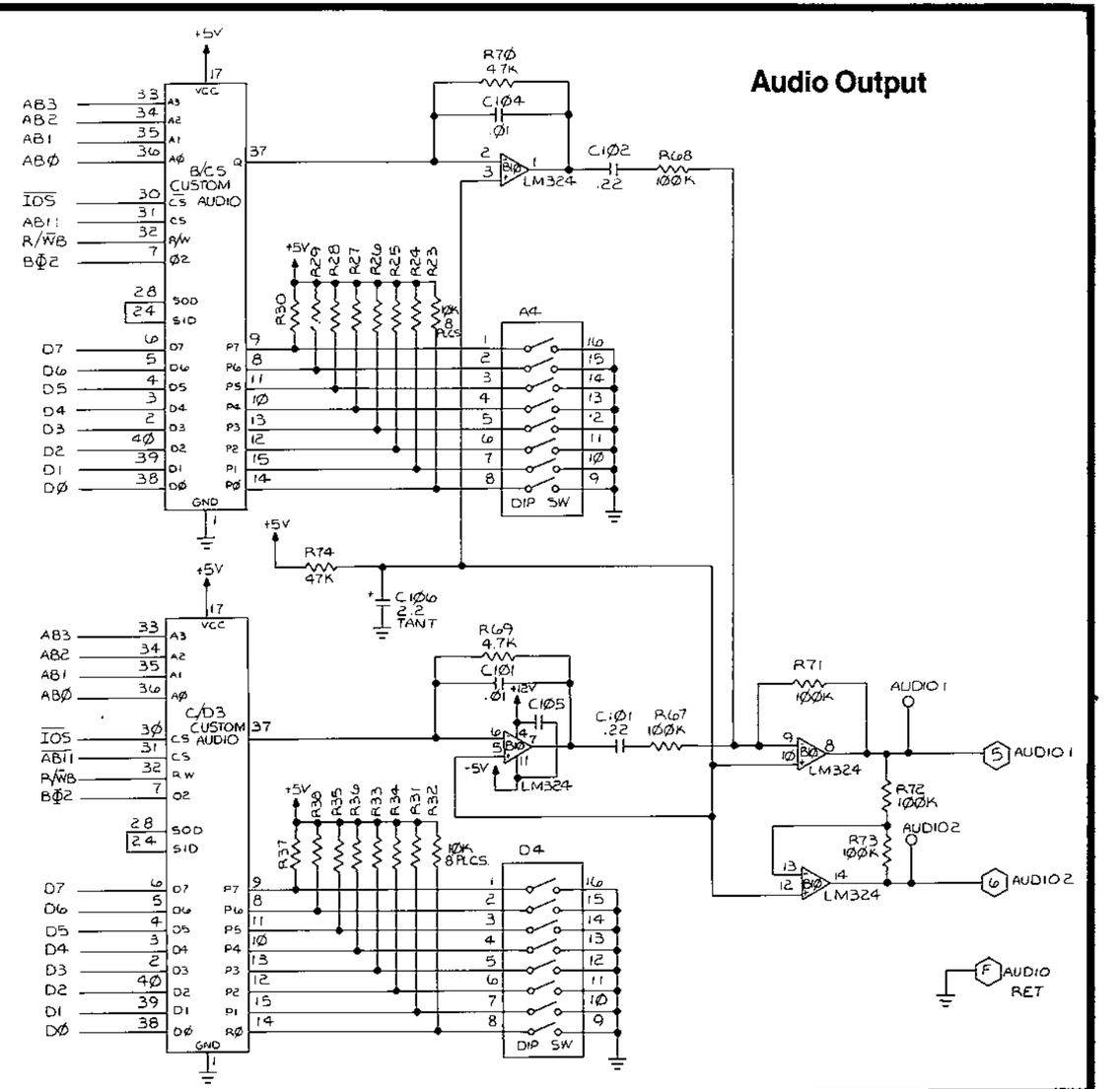
Color Output



Coin Door and LED Output



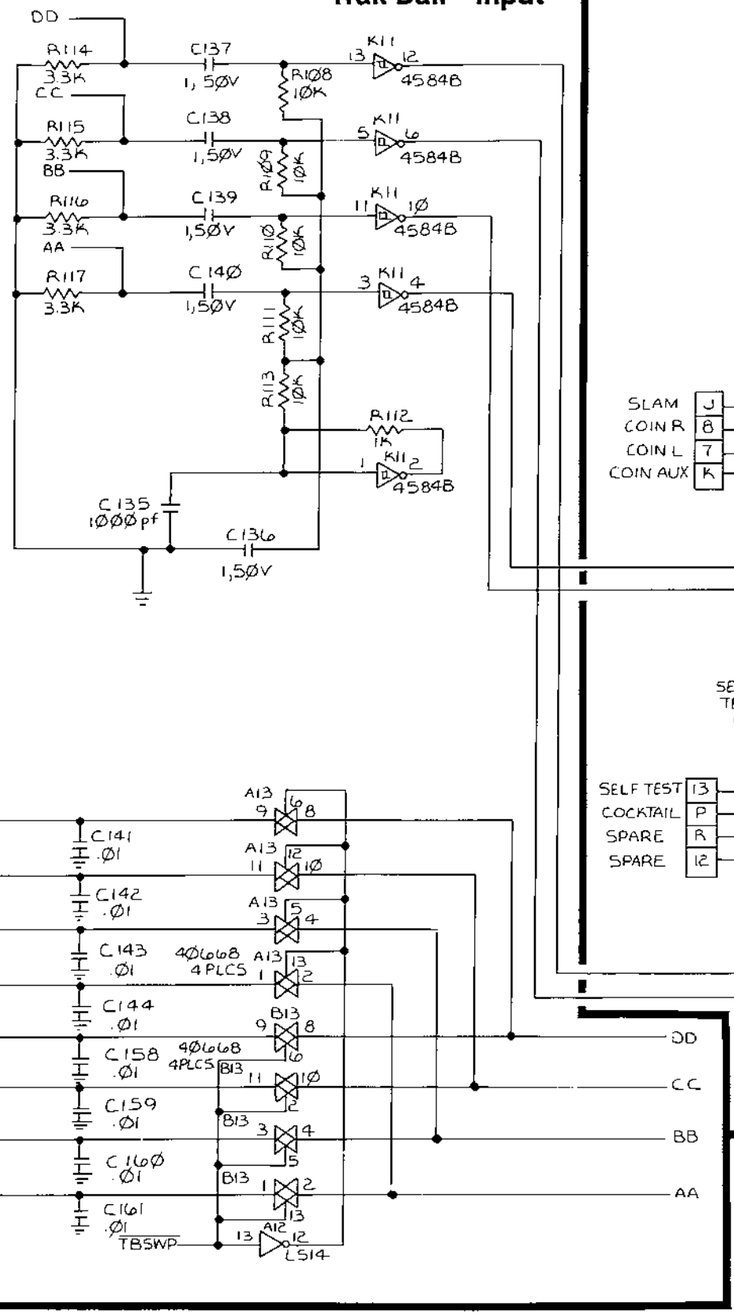
Audio Output



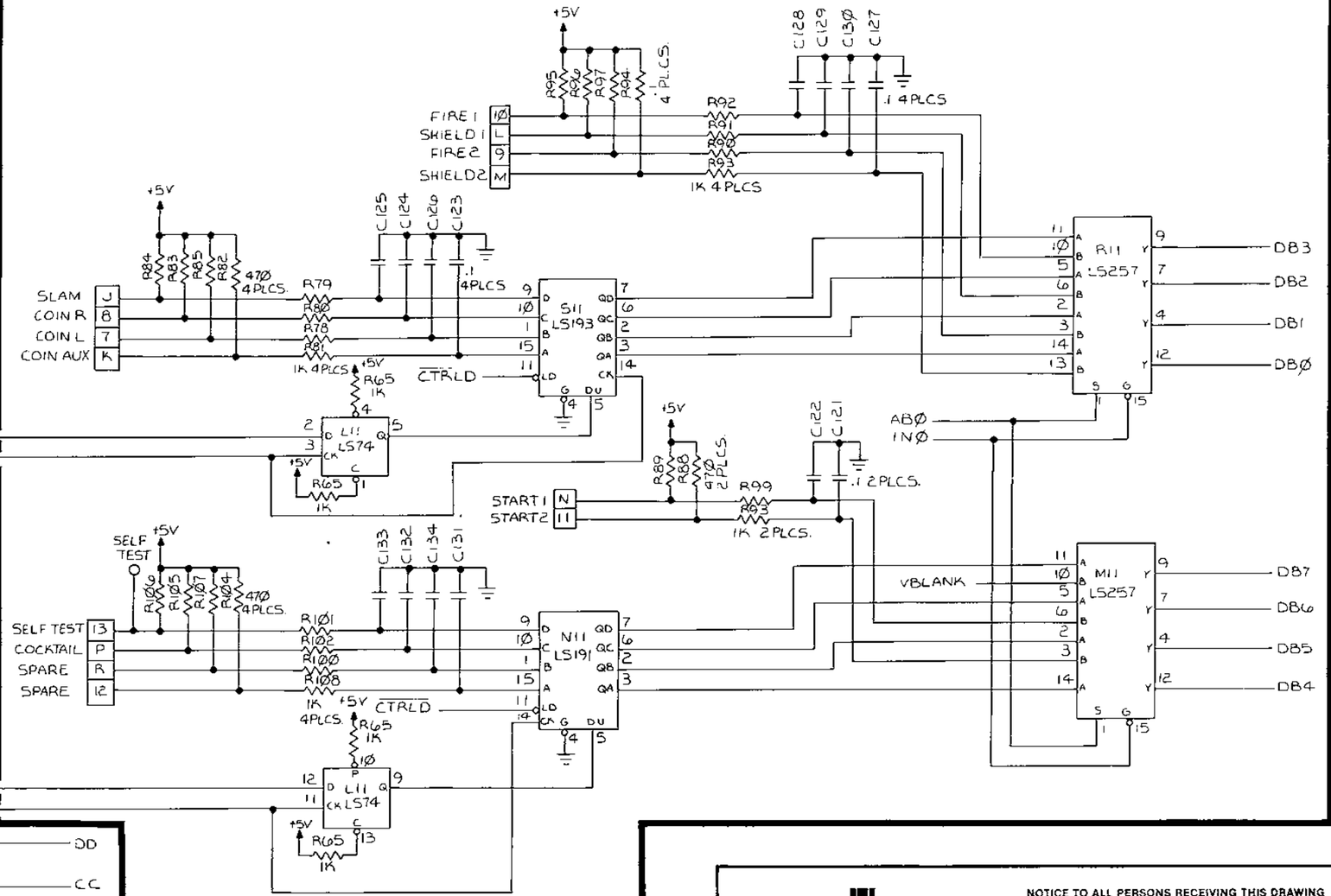
Liberator™ PCB Schematic Diagram

SP-209 Sheet 8B
1st Printing

Trak-Ball™ Input



Coin Door and Control Panel Input



Liberator™ PCB Schematic Diagram

Description of Liberator PCB Signal Names

A0-A15

Address bits on Microprocessor Address Bus lines A0-A15 are software-generated by Microprocessor C2. When BITMD is low, A0-A13 are applied through buffers B1 and E1 to produce the bits on AB0-AB13.

AB0-AB13, $\overline{AB11}$

Address bits on Buffered Microprocessor Address Bus lines AB0-AB13 are software-generated either by Microprocessor C2 or by Bit Map Decoders H1 and F1. When BITMD is low, bits AB0-AB13 are generated via buffers B1 and E1. When BITMD is high and $\overline{BITMD}$ is low, Bit Map Decoders H1 and F1 generate the bits on lines AB0-AB13.

In the Address Decoders circuit, bits on lines AB12 and AB13 are the input signals for decoders T2, T3, and E4; and bits on lines AB9-AB11 are input signals for decoder S2.

Lines AB0-AB11 carry the addresses for the Program Memories.

AB11 is inverted by gate F4 to produce AB11. AB11 is a control bit for custom audio chip B/C3 in the Audio Output circuit. $\overline{AB11}$ is a control bit for custom audio chip C/D3 in the Audio Output circuit.

The Bit Map Address Multiplexers use the bits on lines AB0-AB13, together with those on 1V-128V and 4H-128H, to produce the address bits for the Bit Map Memories. The Bit Map Memory address bits are software-generated by Bit Map Address Multiplexers L9, K9, J9, and H9. When 2H and BMASEL are both low, these address bits are derived from the bits on 2V-128V. When 2H is low and BMASEL is high, the address bits are derived from 4H-128H and 1V. When 2H is high and BMASEL is low, these address bits are derived from AB7-AB13. When both 2H and BMASEL are high, these address bits are from AB0-AB6.

The Base RAM circuit uses the bits on lines AB0-AB3, together with those on 8V-128V, to produce address bits A1-A4 for Base RAM L5.

The Color Memory circuit uses the bits on lines AB0-AB3, together with those on PLAVID0-PLAVID3 and BIT0-BIT2, to produce the address bits for the Color Memories. In addition, the bit on AB4 is gated with $\overline{COLORAM}$ by gate F5 to produce the chip select signals for the Color Memories.

The EAROM circuit uses the bits on lines AB0-AB5 to produce the address bits for EAROM M2.

AUDIO1-AUDIO2

The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B/C3 and C/D3 of the Audio Output circuit. AUDIO1 is the inverse of AUDIO2. These signals are applied to the Audio/Regulator II PCB to ultimately drive speakers 1 and 2.

$\overline{BASRAM}$

The Base RAM Enable signal is software-generated at pin 1 of Address Decoder S2 during addresses 0003 through 033F. $\overline{BASRAM}$ is the select signal for the Base RAM circuit.

BIT0-BIT2

The Pixel Bits on lines BIT0-BIT2 are generated from the Bit Map Shift Registers. When LDRAST is high and the Bit Map Shift Registers receive the next clock pulse, BIT0 is generated at pin 12 of R9 from the data bits on DRAM0-DRAM3; BIT1 is generated at pin 12 of P9 from the data bits on DRAM4-DRAM7; and BIT2 is generated at pin 12 of M9 from the data bits on DRAM8-DRAM11. BIT0-BIT2 are used by the Color Memory circuit to produce the address for the Color Memories.

$\overline{BITMD}$

The Bit Mode Enable signal is software-generated at pin 6 of Bit Map Address Decoder E4 during address 0002. $\overline{BITMD}$ is the output control signal for Bit Map Decoders H1 and F1. When $\overline{BITMD}$ goes low, the data bits latched by H1 and F1 from DB0-DB7 on the last positive-going transitions of XCOORD and YCOORD, are placed on lines AB0-AB13 and PIX0-PIX1.

BITMD

The Bit Mode Disable signal is software-generated at pin 8 of inverter F4 in the Bit Map Address Decoders circuit during address 0002. BITMD is the disenable signal for buffers B1 and E1 of the Microprocessor circuit. When BITMD goes high, the buffers are tri-stated and the bit map addresses are put on the address bus.

BLU

The Blue Signal is a game PCB output signal developed from the bits on B1 and B2. BLU is generated at the emitter of Q4 in the Color Output circuit. The bits on B1 and B2 are summed at the base of Q5 and buffered by Q5 and Q4 to produce BLU.

BMASEL

The Bit Map Address Select signal is hardware-generated at pin 5 of latch E8 in the Refresh circuit. In the Bit Map Address Multiplexers circuit, BMASEL is the A select signal for Bit Map Address Multiplexers H9, J9, K9, and L9.

BΦ2

The active high-level Phase 2 Clock signal is hardware-generated from the internal clock circuitry of Microprocessor C2 and buffered by E3. BΦ2 is gated with $\overline{R}$/WB and $\overline{1H}$ to produce $\overline{WRITE}$. BΦ2 is also used as the clock for custom audio chips B/C3 and C/D3 of the Audio Output circuit.

B/W

The Black and White Video signal is a game PCB output signal that is generated at the emitter of Q11 in the Color Output circuit from $\overline{COMPSYNC}$, BLU, GRN, and RED. This signal can be used by a black and white video display when a color display is not available.

$\overline{CAS}$

The active low-level Column Address Select signal is hardware-generated at pin 9 of latch C9 in the Refresh circuit. $\overline{CAS}$ is used to refresh the column address of the dynamic Bit Map Memories.

CC0-CC3

The bits on Planet Color Code lines CC0-CC3 are software-generated by Planet Picture ROMs P8 and M/N8.

CLRLDWE

The Clear/Load/Write Enable signal is hardware-generated at pin 9 of latch C8 in the Multiply Clock circuit. CLRLDWE is a control signal for the Multiply Clock circuit.

COINCNTRL

The Coin Counter Left signal is a game PCB output signal generated at the collector of Q3 in the Coin Door and Utility Panel Output circuit. COINCNTRL is applied to the game utility panel to activate the Left Coin Counter.

COINCNTRR

The Coin Counter Right signal is a game PCB output signal generated at the collector of Q2 in the Coin Door and Utility Panel Output circuit. COINCNTRR is applied to the game utility panel to activate the Right Coin Counter.

$\overline{COLORAM}$

The active low-level Color RAM Enable signal is software-generated at pin 2 of Address Decoder S2 during addresses 6200 through 621F and is used in the Color Memory circuit. When $\overline{COLORAM}$ is low, the Color Memory address bits are from AB0-AB3. When $\overline{COLORAM}$ is high and the A select signal is low, the Color Memory address bits are from BIT0-BIT2. When $\overline{COLORAM}$ and the A select signal are high, the Color Memory Address bits are from PLAVID0-PLAVID3. When both $\overline{COLORAM}$ and 5MHZ go low, the Color Memories are enabled to write data.

$\overline{COMPSYNC}$

The active low-level Composite Synchronization signal is hardware-generated at pin 3 of gate M3 in the Vertical Sync Chain by exclusive-ORing $\overline{HSYNC}$ and VSYNC. $\overline{COMPSYNC}$ is applied directly to the video display circuitry for further processing.

$\overline{CTRLD}$

The active low-level Control Load signal is generated at pin 9 of latch T11 in the Coin Counter and LED Output circuit. When $\overline{CTRLD}$ goes low, counters S11 and N11 are loaded from the Coin Door and Control Panel Input switches.

D0-D7

Microprocessor Data Bus lines D0-D7 form a bidirectional data bus between the Microprocessor, the Program Memory, and the Audio Output circuits.

DB0-DB7

Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered bidirectional data bus between microprocessor data-bus buffer E2 and Bit Map Decoders H1 and F1; Bit Map Data Multiplexers H11 and P11; Bit Map Data Buffers T9, S9, and N9; Bit Map Memories H10, R10, N10, and K10; Longitude Scaling latch R6; Color Memories F11, C11, E11, and B11; EAROM latches R2 and K2; EAROM buffer H2; Coin Door and LED Output decoder T11; and Coin Door and Control Panel Input multiplexers R11 and M11.

DINIT

The active high-level Display Initialize signal is generated at pin 8 of gate L4 in the Planet ROM Address Generator circuit. When high, DINIT clears counter M7 and (via gate F5) clears latch E5. In the Line Buffer Address Controller circuit, DINIT clears flip-flop K4 and counter H7.

$\overline{DISDAT}$

Disable Data is an active low-level signal generated by test equipment connected to the $\overline{DISDAT}$ test point.

DRAM0-DRAM11

The bits on Bit Map Data Bus lines DRAM0-DRAM11 are software-generated by the Bit Map Memories. When BITMD, $\overline{RAM}$, and $\overline{R}$/WB are all low, the bits on DRAM0-DRAM7 are passed through Bit Map Data Buffer T9 to the microprocessor data bus. Otherwise, when $\overline{BITMD}$ and $\overline{R}$/WB are low, the bits on DRAM0-DRAM11 are multiplexed by S9 and N9 of the Bit Map Data Buffer circuit and passed to lines DB4-DB7 of the microprocessor data bus.

In the Bit Map Shift Registers circuit, if LDRAST is high, the bits on DRAM0-DRAM3 are used by shift register R9 to produce BIT0; the bits on DRAM4-DRAM7 are used by shift register P9 to produce BIT1; and the bits on DRAM8-DRAM11 are used by shift register M9 to produce BIT2.

EARCON

The Electrically Alterable Read-Only Memory Control signal is software-generated at pin 4 of Address Decoder S2 at address 6600. EARCON is the clock signal for latch R2 in the EAROM circuit. When high, EARCON allows R2 to pass data bits on lines DB0-DB3 to the control lines of EAROM M2.

$\overline{EARD}$

The Electrically-Alterable Read-Only Memory Read Enable is software-generated at pin 12 of Address Decoder E4 at address 4000. $\overline{EARD}$ is the select signal for buffer H2 of the EAROM circuit. When low, $\overline{EARD}$ allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

$\overline{EARWR}$

The Electrically-Alterable Read-Only Memory Write Enable is software-generated at pin 9 of Address Decoder S2 at addresses 6E00 through 6E3F. $\overline{EARWR}$ is the clock signal for latches P2 and K2 in the EAROM circuit. When low, $\overline{EARWR}$ allows address bits on lines AB0-AB5 and data bits on lines DB0-DB7 to pass to the address and data input pins of EAROM M2.

FSG

The active high-level First Segment signal is the carry output of adder R7 in the Longitude Scaling circuit. When FSG is high and LDRAST is high, the C0 input of adder P7 is set high. In addition, FSG is gated with PLS and HOR by gates R4, R3, and P3 in the Planet ROM Address Generator circuit to produce the clock signal for latch N7.

Liberator™ PCB Signal Name Descriptions

Description of Liberator PCB Signal Names (continued)

GRN

The Green signal is a game PCB output signal developed from the bits on G0-G2. GRN is generated at the emitter of Q8 in the Color Output circuit. The bits on G0-G2 are summed at the base of Q9 and buffered by Q8 and Q9 to produce GRN.

HBLANK

The active high-level Horizontal Blanking signal is hardware-generated at pin 11 of counter F9 in the Horizontal Sync Chain. HBLANK is applied through inverter L3 to produce $\overline{\text{HBLANK}}$. If HBLANK is high when latch T4 is clocked, HBLANK* is set high and $\overline{\text{HBLANK}}$* is set low. When HBLANK goes low, HSYNC from latch T4 is preset to the high state.

$\overline{\text{HBLANK}}$

The active low-level Horizontal Blanking signal is hardware-generated at pin 6 of inverter L3 in the Horizontal Sync Chain by inverting HBLANK. When low, $\overline{\text{HBLANK}}$ presets HBLANK* from latch T4 to the low state and $\overline{\text{HBLANK}}$* to the high state. In the Planet Control circuit, when $\overline{\text{HBLANK}}$ goes low, it presets $\overline{\text{HOR}}$ from latch S3 to the high state and HOR to the low state.

HBLANK*

The active high-level Delayed Horizontal Blanking signal is hardware-generated at pin 9 of latch T4 in the Horizontal Sync Chain. HBLANK* is generated when HBLANK has been delayed by the gated result of 8H and 10MHZ. HBLANK* is the clock signal for latch M4 in the Vertical Sync Chain.

$\overline{\text{HBLANK}}$*

The active low-level Delayed Horizontal Blanking signal is hardware-generated at pin 8 of latch T4 in the Horizontal Sync Chain. $\overline{\text{HBLANK}}$* is generated when HBLANK has been delayed by the gated result of 8H and 10MHZ. $\overline{\text{HBLANK}}$* is the clock signal for latch L8 in the Vertical Sync Chain. In the Valid Segment Detector, $\overline{\text{HBLANK}}$* is gated with $\overline{\text{HORDL}}$ by gate P3 to produce the clock signal for latch N3. When $\overline{\text{HBLANK}}$* goes low, counters B6 and D6 in the Display Counter and Comparator circuit are enabled to load data.

HCLK1, HCLK2

The Trak-Ball™ Horizontal Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, HCLK1 is the clock signal for latch L11 and counter S11 in the Coin Door and Control Panel Input circuit; when $\overline{\text{TBSWP}}$ is low, HCLK2 is the clock signal for latch L11 and counter S11.

HDIR1, HDIR2

The Trak-Ball™ Horizontal Direction signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, HDIR1 enables counter S11 in the Coin Door and Control Panel Input circuit to count; when $\overline{\text{TBSWP}}$ is low, HDIR2 enables counter S11.

HOR

The Horizontal Planet Enable signal is hardware-generated at pin 6 of latch S3 in the Planet Control circuit. When HBLANK goes low, HOR is preset to the low state. When latch S3 receives the next positive-going transition of clock 64H, HOR is set high. HOR is latched by S4 during the next positive-going transition of LDRAST to produce HORDL and $\overline{\text{HORDL}}$.

$\overline{\text{HOR}}$

The Complementary Horizontal Planet Enable signal is hardware-generated at pin 5 of latch S3 in the Planet Control circuit. When $\overline{\text{HBLANK}}$ goes low, $\overline{\text{HOR}}$ is preset to the high state. When latch S3 receives the next positive-going transition of clock 64H, $\overline{\text{HOR}}$ is set low. In the Planet ROM Address Generator circuit, when $\overline{\text{HOR}}$ goes high, it is gated with HORDL by gate P4 to produce the load signal for counter M7. In the Valid Segment Detector circuit, $\overline{\text{HOR}}$ is the clear signal for latch N3.

HORDL

The active high-level Delayed Horizontal Planet Enable signal is hardware-generated at pin 7 of latch S4 in the Planet Control circuit. HORDL is HOR which has been delayed by one cycle of LDRAST. HORDL, 2H, 1H, and all remaining output signals from latch S4 are gated by M3, M5, and N4 to produce PLANET, PLANETDL, and PLANETDL from latches D9 and H5. In the Planet ROM Address Generator circuit, when HORDL goes high, it is gated with $\overline{\text{HOR}}$ by gate P4 to produce the load signal for counter M7. In the Line Buffer Address Controller circuit, HORDL and 4H are used by latch S3 and gate J3 to produce PINIT2.

$\overline{\text{HORDL}}$

The Complementary Delayed Horizontal Planet Enable signal is hardware-generated at pin 6 of latch S4 in the Planet Control circuit. $\overline{\text{HORDL}}$ is the complement of HOR. HORDL, 2H, 1H, and all remaining output signals from latch S4 in the Planet Control circuit are used to produce PLANET, PLANETDL, and PLANETDL. When high, $\overline{\text{HORDL}}$ is gated with HOR by gate L4 in the Planet ROM Address Generator circuit to produce DINIT. When low, $\overline{\text{HORDL}}$ is gated with $\overline{\text{HBLANK}}$* by gate P3 in the Valid Segment Detector circuit to produce the clock signal for latch N3.

HSYNC

The Horizontal Synchronization signal is hardware-generated at pin 6 of latch T4 in the Horizontal Sync Chain. HSYNC is generated from 32H when latch T4 is clocked by 16H. HSYNC is the clock signal for counters H8 and J8 in the Vertical Sync Chain. HSYNC is also applied directly to the video display circuitry for further processing.

$\overline{\text{HSYNC}}$

The Complementary Horizontal Synchronization signal is hardware-generated at pin 5 of latch T4 in the Horizontal Sync Chain. HSYNC is generated from 32H when latch T4 is clocked by 16H. HSYNC is exclusive-ORed with VSYNC by gate M3 in the Vertical Sync Chain to produce $\overline{\text{COMPSYNC}}$.

$\overline{\text{IN0}}$

The active low-level Input Switch 0 Enable signal is software-generated at pin 11 of Address Decoder E4 at addresses 5000 through 5001. $\overline{\text{IN0}}$ is the output control enable signal for multiplexers R11 and M11 in the Coin Door and Control Panel Input circuit.

$\overline{\text{INTACK}}$

The active low-level Interrupt Acknowledge signal is software-generated at pin 3 of Address Decoder S2 at address 6400. This signal is an acknowledgment from Microprocessor C2 that an interrupt request has been received. INTACK presets latch K3.

$\overline{\text{IOS}}$

The active low-level Input/Output Sound signal is software-generated at pin 9 of Address Decoder E4 during addresses 7000 through 781F. In the Microprocessor circuit, $\overline{\text{IOS}}$ is gated with the ROM signal by gates H4 and H3 to enable bidirectional data bus buffer E2 to pass data. When $\overline{\text{IOS}}$ or ROM is high, data buffer E2 is turned off, which allows custom audio chips B/C3 and C/D3 to pass data to the microprocessor data bus.

IRQCK

The active high-level Interrupt Request Clock is hardware-generated at pin 15 of latch M4 in the Vertical Sync Chain. IRQCK is the interrupt clock signal for Microprocessor C2.

LATCHEN

The active high-level Latch Enable is generated at pin 1 of gate B9 in the Display Counter and Comparator circuit. LATCHEN is the clock signal for latch A6 in the Display Counter and Comparator circuit and for latch P5 in the Line Buffer circuit.

LBAINC

The active high-level Line Buffer Address Increment signal is generated at pin 10 of J-K flip-flop K4 in the Display Counter and Comparator circuit. In the Line Buffer Address Controller circuit, when LBAINC is high and if either $\overline{\text{VASEG}}$ or LDRAST is high, J-K flip-flop K4 is clocked and counter H7 is enabled to count.

LDRAST

The active high-level Load Raster Enable signal is hardware-generated at pin 6 of Load Raster Control Latch K3. When high, LDRAST is the shift/load signal for Bit Map Shift Registers R9, P9, and M9; the clock signal for latch S4 in the Planet Control circuit; and the clock signal for latch S3 in the Line Buffer Address Controller circuit.

LGS0-LGS7

The Longitude Scaling bits on lines LGS0-LGS7 are software-generated by Longitude Scalers T7 and S7. These bits are developed from the output signals of the Planet Picture ROMs and the latched data bits from R6. The bits on LGS0-LGS7, together with those from Latitude Scalers P6 and N6, are used by the Multiplier circuit to produce the bits on lines X0-X7.

LX0-LX7, $\overline{\text{LXD2}}$-$\overline{\text{LXD3}}$

The bits on Display Segment Length lines LX0-LX7 are software-generated from Line Buffer RAMs B7, C7, D7, and E7. In the Valid Segment Detector, LX0- LX7 are used to produce $\overline{\text{VASEG}}$. In addition, the bits on LX2 and LX3 are applied to latch P5 to produce the delayed bits of $\overline{\text{LXD2}}$ and $\overline{\text{LXD3}}$.

In the Display Counter and Comparator circuit, the bits on LX0-LX1, LX4-LX7, and $\overline{\text{LXD2}}$-$\overline{\text{LXD3}}$ are applied to comparators C6 and E6.

MD0-MD7

The data bits on Multiplexed Data bus lines MD0-MD7 are generated by Bit Map Data Multiplexers H11 and P11 from the data bits on DB0-DB7. When $\overline{\text{BITMD}}$ goes high, H11 and P11 multiplex the data bits from DB0-DB7 to produce those on MD0-MD7. Bit Map Memories E10, T10, P10, L10, F10, S10, M10, and J10 use the data on lines MD0-MD7 to generate DRAM0-DRAM7.

$\overline{\text{MTR}}$

The Multiplier signal is generated at pin 7 of shift register S6 in the Multiplier circuit. $\overline{\text{MTR}}$ is the shift/load enable for shift registers K6 and J6.

MULCLK

The active high-level Multiply Clock signal is hardware-generated at pin 8 of gate J4 in the Multiply Clock circuit. MUCLK is the clock signal for shift register S6, latch H5, and decoders K5 and J6 in the Multiplier circuit.

$\overline{\text{OUT0}}$

The active low-level Output Port 0 signal is software-generated at pin 7 of Address Decoder S2 at address 6C00. $\overline{\text{OUT0}}$ is the enable signal for decoder T11 in the Coin Counter and LED Output circuit.

$\overline{\text{PINIT2}}$

The active low-level Process Initialize signal is generated at pin 6 of gate J3 in the Line Buffer Address Controller circuit. If HORDL and 4H are low when LDRAST goes high, $\overline{\text{PINIT2}}$ is set low. $\overline{\text{PINIT2}}$ loads counter H7 and presets flip-flop K4 in the Line Buffer Address Controller. In the Multiplier circuit, $\overline{\text{PINIT2}}$ clears latches F6 and D10. In the Valid Segment Detector, $\overline{\text{PINIT2}}$ clears latch N3.

PIX0

The active high-level Pixel Bit 0 is software-generated at pin 9 of Bit Map Decoder F1 from the bit on DB0. In the Write Protection circuit, PIX0 and PIX1 are multiplexed by C5 to produce $\overline{\text{WP0}}$. In the Bit Map Data Buffers circuit, PIX0 is the A select signal for multiplexers S9 and N9.

PIX1

The active high-level Pixel Bit 1 is software-generated at pin 6 of Bit Map Decoder F1 from the bit on DB1. In the Write Protection circuit, PIX1 and PIX0 are multiplexed by C5 to produce $\overline{\text{WP0}}$. In the Bit Map Data Buffers circuit, PIX1 is the B select signal for multiplexers S9 and N9.

PLA1

The Planet 1 Select signal is generated at pin 12 of latch T11 in the Coin Counter and LED Output circuit from the data bit on DB4. PLA1 is the chip select signal for Planet Picture ROMs M/N8 and T8.

ATARI®

Liberator™ PCB Signal Name Descriptions

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Description of Liberator PCB Signal Names (continued)

PLA2

The Planet 2 Select signal is generated at pin 2 of inverter L3 in the Coin Counter and LED Output circuit by inverting PLA1. PLA2 is the chip select signal for Planet Picture ROMs P8 and R/S8.

PLANET

The Planet Enable signal is generated at pin 6 of flip-flop D9 in the Planet Control circuit. PLANET changes states at a 5-MHz rate if either of the signals at pins 2 or 3 of D9 is high. When high, PLANET is used by latch H5 to produce PLANETDL and $\overline{\text{PLANETDL}}$. When low, PLANET clears flip-flop K4 in the Display Counter and Comparator circuit.

PLANETDL

The active high-level Delayed Planet Enable signal is generated at pin 9 of latch H5 in the Planet Control circuit. When PLANETDL is high and counter D6 of the Display Counter and Comparator circuit has reached its minimum count, gate P4 produces the enable signal for Counter B6. At this time, if counter B6 was previously loaded by $\overline{\text{HBLANK}}$* going low, counter B6 begins counting down.

$\overline{\text{PLANETDL}}$

The Complementary Delayed Planet Enable signal is generated at pin 8 of latch H5 in the Planet Control circuit. $\overline{\text{PLANETDL}}$ is the enable signal for Counter D6 in the Display Counter and Comparator circuit. When PLANETDL goes low, counter D6 begins counting down. In the Color Memory circuit, $\overline{\text{PLANETDL}}$ is gated by N5 with the latched BIT0–BIT2 outputs from R5 by gate N5 to produce the input signal for latch D5.

PLAVID0–PLAVID3

The Planet Video signals are software-generated by Line Buffers J7 and K7, latched by P5, and applied through multiplexers S5 and T5 to produce the Color Memory address bits.

PLS

The active high-level Planet Segment signal is hardware-generated at pin 8 of latch C8 in the Multiply Clock circuit. In the Planet ROM Address Generator circuit, PLS is gated with FSG and HOR by gates R4, R3, and P3 to produce the clock signal for latch N7. In the Multiplier circuit, PLS is the clock signal for latches F6 and D10.

$\overline{\text{RAM}}$

The active low-level Random-Access Memory enable is software-generated at pin 4 of Address Decoder T2. $\overline{\text{RAM}}$ is gated with A2–A13 by gates D1 and C1 of the Bit Map Address Decoders to produce the enable signal for E4. In the Write Protection circuit, $\overline{\text{RAM}}$ is gated with WRITE to produce the clear signal for latch D5. In the Bit Map Data Buffer circuit, $\overline{\text{RAM}}$ is gated with BITMD and R/$\overline{\text{WB}}$ by gate F3 to produce the enable signal for buffer T9.

$\overline{\text{RAS}}$

The active low-level Row Address Select signal is hardware-generated at pin 9 of latch E8 in the Refresh circuit. $\overline{\text{RAS}}$ is used to refresh the row address of the dynamic Bit Map Memories.

RED

The Red signal is a game PCB output signal developed from the bits on R0– R2. RED is generated at the emitter of Q6 in the Color Output circuit. The bits on R0–R2 are summed at the base of Q7 and buffered by Q7 and Q6 to produce RED.

$\overline{\text{RESET}}$

Reset is an active low-level signal generated at pin 12 of counter J11 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets $\overline{\text{RESET}}$ to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regulated levels. This ensures that the Microprocessor Address Bus (A0–A15) is stabilized before Microprocessor C2 begins operation.

The Watchdog circuit sets $\overline{\text{RESET}}$ to an active low level if the microprocessor fails to output address before counter J11 has reached its maximum count.

$\overline{\text{RESET}}$ is the clear signal for latches R2 in the EAROM circuit and T11 in the Coin Counter and LED Output circuit.

ROM

The active high-level Read-Only Memory Enable signal is software-generated at pin 8 of gate H4 in the Address Decoders circuit during addresses 8000 through EFFF. In the Microprocessor circuit, ROM is gated with $\overline{\text{I/OS}}$ by gates H4 and H3 to enable bidirectional data-bus buffer E2 to pass data.

In addition, ROM is ANDed with $\overline{\text{DISDAT}}$ by gate H4 in the Program Memory circuit to enable buffer F2 to pass data.

$\overline{\text{ROM0}}$

The active low-level Read-Only Memory Chip Select 0 signal is software-generated at pin 12 of Address Decoder T3 during addresses 8000 through 8FFF. $\overline{\text{ROM0}}$ is the chip-select signal for Program Memory J1. When low, $\overline{\text{ROM0}}$ allows J1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM1}}$

The active low-level Read-Only Memory Chip Select 1 signal is software-generated at pin 11 of Address Decoder T3 during addresses 9000 through 9FFF. $\overline{\text{ROM1}}$ is the chip-select signal for Program Memory K/L1. When low, $\overline{\text{ROM1}}$ allows K/L1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM2}}$

The active low-level Read-Only Memory Chip Select 2 signal is software-generated at pin 10 of Address Decoder T3 during addresses A000 through AFFF. $\overline{\text{ROM2}}$ is the chip-select signal for Program Memory L/M1. When low, $\overline{\text{ROM2}}$ allows L/M1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM3}}$

The active low-level Read-Only Memory Chip Select 3 signal is software-generated at pin 9 of Address Decoder T3 during addresses B000 through BFFF. $\overline{\text{ROM3}}$ is the chip-select signal for Program Memory N1. When low, $\overline{\text{ROM3}}$ allows N1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM4}}$

The active low-level Read-Only Memory Chip Select 4 signal is software-generated at pin 12 of Address Decoder T2 during addresses C000 through CFFF. $\overline{\text{ROM4}}$ is the chip-select signal for Program Memory P/R1. When low, $\overline{\text{ROM4}}$ allows P/R1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM5}}$

The active low-level Read-Only Memory Chip Select 5 signal is software-generated at pin 11 of Address Decoder T2 during addresses D000 through DFFF. $\overline{\text{ROM5}}$ is the chip-select signal for Program Memory R/S1. When low, $\overline{\text{ROM5}}$ allows R/S1 to be addressed and to pass data to buffer F2.

$\overline{\text{ROM6}}$

The active low-level Read-Only Memory Chip Select 6 signal is software-generated at pin 8 of gate P3 in the Address Decoder circuit during addresses E000 through EFFF. $\overline{\text{ROM6}}$ is the chip-select signal for Program Memory T1. When low, $\overline{\text{ROM6}}$ allows T1 to be addressed and to pass data to buffer F2.

R/$\overline{\text{WB}}$

The Buffered Read(High)/Write(Low) Enable signal is generated at pin 10 of inverter F4 in the Microprocessor circuit. R/$\overline{\text{WB}}$ is gated with BΦ2 and 1H by gates H4 and J4 to produce $\overline{\text{WRITE}}$. In the Bit Map Data Buffers circuit, R/$\overline{\text{WB}}$ is gated with $\overline{\text{RAM}}$, BITMD, and $\overline{\text{BITMD}}$ by gate F3 to produce the enable signals for buffer T9 and multiplexers S9 and N9.

R/$\overline{\text{WB}}$

The Buffered Read(High)/Write(Low) Enable signal is generated by Microprocessor C2, buffered by E3, and applied to custom audio chips B/C3 and C/D3 of the Audio Output circuit and buffer E2 of the Microprocessor circuit. R/$\overline{\text{WB}}$ determines the direction of data flow through these devices.

SGC0–SGC4

The Planet Segment Code bits on lines SGC1–SGC4 are hardware-generated by counter M7 in the Planet ROM Address Generator circuit. The bit on line SGC0 is hardware-generated at pin 5 of latch E5. The Planet Segment Code provides the address bits for the Planet Picture ROM.

STARTLG

The active high-level Starting Longitude Enable signal is software-generated at pin 5 of Address Decoder S2 at address 6800. STARTLG is the clock signal for latch R6 in the Longitude Scaling circuit.

$\overline{\text{VASEG}}$

The active low-level Valid Segment signal is generated at pin 9 of latch N3 in the Valid Segment Detector. When the carry bit from adder F7 is set high and 2H is high, $\overline{\text{VASEG}}$ is set low on the next positive-going transition of 1H. $\overline{\text{VASEG}}$ is gated with LDRAST and LBAINC by gates N4 and J4 to clock flip-flop K4 and enable a count-up operation by counter H7.

VBLANK

The active high-level Vertical Blanking signal is hardware-generated at pin 11 of latch M4 in the Vertical Sync Chain. VBLANK is applied to multiplexer M11 in the Coin Door and Control Panel Input circuit. When IN0 is low and AB0 is high, VBLANK is read by Microprocessor C2 on data bus line DB7.

$\overline{\text{VBLANK}}$

The active low-level Vertical Blanking signal is hardware-generated at pin 10 of latch M4 in the Vertical Sync Chain. $\overline{\text{VBLANK}}$ is gated with $\overline{\text{HBLANK}}$* by gate L4 of the Horizontal Sync Chain to produce $\overline{\text{VIDBLANK}}$.

VCLK1, VCLK2

The Trak-Ball™ Vertical Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, VCLK1 is the clock signal for latch L11 and counter N11 in the Coin Door and Control Panel Input circuit; when $\overline{\text{TBSWP}}$ is low, VCLK2 is the clock signal for latch L11 and counter N11.

VDIR1, VDIR2

The Trak-Ball™ Vertical Direction signals are PCB input signals to the Trak-Ball™ Input circuit. When $\overline{\text{TBSWP}}$ is high, VDIR1 enables counter N11 in the Coin Door and Control Panel Input circuit to count; when $\overline{\text{TBSWP}}$ is low, BDIR2 enables counter N11.

$\overline{\text{VIDBLANK}}$

The active low-level Video Blanking signal is hardware-generated at pin 6 of gate L4 in the Horizontal Sync Chain. $\overline{\text{VIDBLANK}}$ is the clear signal for Color Memory latches A11 and D11.

$\overline{\text{VPLA}}$

The active low-level Vertical Planet Enable signal is hardware-generated at pin 2 of latch M4 in the Vertical Sync Chain. $\overline{\text{VPLA}}$ is gated with PSIG2 by gate R4 in the Planet Control circuit to produce the clear signal for latch D9.

VSYNC

The active high-level Vertical Synchronization signal is hardware-generated at pin 6 of latch M4 in the Vertical Sync Chain. VSYNC is exclusive-ORed with $\overline{\text{HSYNC}}$ by gate M3 to produce $\overline{\text{COMPSYNC}}$. VSYNC is also applied directly to the video display circuitry for further processing.

$\overline{\text{WDDIS}}$

Watchdog Disable is a test point at pin 1 of gate L4 in the Watchdog circuit. When $\overline{\text{WDDIS}}$ is grounded, $\overline{\text{RESET}}$ is prevented from going to an active low level (except when the RESET test point is grounded).

Liberator™ PCB Signal Name Descriptions

Description of Liberator PCB Signal Names (continued)

WDOG

The active low-level Watchdog signal is software-generated at pin 6 of Address Decoder S2. WDOG is gated with WDDIS by gate L4 in the Watchdog circuit to produce the load signal for counter J11 of the Power-On Reset circuit.

WP0-WP3

The active low-level Write Pulses 0-3 are software-generated from gate B5 in the Write Protection circuit. These pulses are the write enable signals for the Bit Map Memories.

WRITE

The active low-level Write Enable signal is hardware-generated at pin 11 of gate J4 in the Microprocessor circuit. WRITE is applied to gate H3 in the Bit Map Address Decoders circuit where it is used to develope YCOORD and XCOORD. In the Write Protection circuit, WRITE is gated with RAM by gate N4 to produce the clear signal for latch D5. In the Address Decoders circuit, WRITE is applied to gate H3 to produce the D input signal for decoder S2.

X0-X7

The Planet Scaling bits are generated by latches F6 and D10 in the Multiplier circuit. These bits are developed by those from the Longitude and Latitude Scaling circuits. In the Valid Segment Detector, the bits on X0-X7 and those on LX0-LX7 are summed to produce VASEG from the carry bit of adder F7.

XCOORD

The active high-level Pixel X Coordinate signal is software-generated at pin 3 of gate H3 in the Bit Map Address Decoders circuit during address 0000. XCOORD is the clock signal for Bit Map Decoder F1. When XCOORD goes high, F1 internally latches the data bits from DB0-DB7. Then, when BITMD goes low, these bits are output from F1 to lines PIX0-PIX1 and AB0-AB5.

YCOORD

The active high-level Pixel Y Coordinate signal is software-generated at pin 11 of gate H3 in the Bit Map Address Decoders circuit during address 0001. YCOORD is the clock signal for Bit Map Decoder H1. When YCOORD goes high, H1 internally latches the data bits from DB0-DB7. Then, when BITMD goes low, these bits are output from H1 to lines AB6-AB13.

1H

Horizontal Timing Signal 1 is hardware-generated at pin 10 of latch D9 in the Horizontal Sync Chain. 1H is ANDed with 5MHZ by gate F8 of the Refresh circuit for use in developing RAS. In the Multiply Clock circuit, 1H is ANDed with 2H by gate F8 to produce the clear signal for latch D8. 1H is the clock signal for latch N3 of the Valid Segment Detector. In the Planet Control circuit, 1H is exclusive-ORed with the output signal at pin 14 of latch S4 by gate M3.

1H

Complementary Horizontal Timing Signal 1 is hardware-generated at pin 9 of latch D9 in the Horizontal Sync Chain. In the Microprocessor circuit, 1H is gated with BΦ2 and R/WB by gates H4 and J4 to produce WRITE. 1H is NANDed with 2H by gate N4 of the Load Raster Control Latch to develop the input signal for latch K3.

2H

Horizontal Timing Signal 2 is hardware-generated at pin 14 of counter E9 in the Horizontal Sync Chain. 2H is applied through inverter A8 to produce 2H. 2H is the timing reference for Microprocessor C2. In the Bit Map Address Multiplexer Circuit, 2H is the B select input for multiplexers L9, K9, J9, and H9. 2H is gated with 1H by gate N4 to produce the input signal for Load Raster Control Latch K3. In the Multiply Clock, 2H is ANDed with 1H by gate F8 to produce the clear signal for latch D8. In the Planet Control circuit, 2H is exclusive-ORed with the output signal at pin 10 of latch S4 by gate M3.

2H

Complementary Horizontal Timing Signal 2 is hardware-generated at pin 10 of inverter A8 in the Horizontal Sync Chain. 2H is the clock signal for latch E5 of the Planet ROM Address Generator. In the Valid Segment Detector, 2H is gated by P4 to produce the input signal for latch N3. 2H is the clock signal for multiplexer K5 in the Base RAM circuit.

4H

Horizontal Timing Signal 4 is hardware-generated at pin 13 of counter E9 in the Horizontal Sync Chain. 4H is applied through inverter A8 to produce 4H. 4H is multiplexed with 2V, AB7, and AB0 by Bit Map Address Multiplexer H9.

4H

Complementary Horizontal Timing Signal 4 is hardware-generated at pin 12 of inverter A8 in the Horizontal Sync Chain. 4H is applied to gate J3 in the Line Buffer Address Controller to produce PINIT2.

8H

Horizontal Timing Signal 8 is hardware-generated at pin 12 of counter E9 in the Horizontal Sync Chain. 8H is ANDed with 10MHZ by gate F8 to produce the clock signal for latch T4 in the Horizontal Sync Chain. 8H is multiplexed with 4V, AB8, and AB1 by Bit Map Address Multiplexer H9.

16H

Horizontal Timing Signal 16 is hardware-generated at pin 11 of counter E9 in the Horizontal Sync Chain. 16H is the clock signal for latch T4 of the Horizontal Sync Chain. 16H is multiplexed with 8V, AB9, and AB2 by Bit Map Address Multiplexer J9.

32H

Horizontal Timing Signal 32 is hardware-generated at pin 14 of counter F9 in the Horizontal Sync Chain. 32H is used by latch T4 of the Horizontal Sync Chain to produce HSYNC and HSYNC. 32H is multiplexed with 16V, AB10, and AB3 by Bit Map Address Multiplexer J9.

64H

Horizontal Timing Signal 64 is hardware-generated at pin 13 of counter F9 in the Horizontal Sync Chain. 64H is multiplexed with 32V, AB11, and AB4 by Bit Map Address Multiplexer K9. In the Planet Control circuit, 64H is the clock signal for latch S3.

128H

Horizontal Timing Signal 128 is hardware-generated at pin 12 of counter F9 in the Horizontal Sync Chain. 128H is multiplexed with 64V, AB12, and AB5 by Bit Map Address Multiplexer K9.

5MHZ

The 5 MHz Clock signal is hardware-generated at pin 5 of Clock latch C9. 5MHZ is the P enable signal for counters E9 and F9 in the Horizontal Sync Chain. In the Refresh circuit, 5MHZ is ANDed with 1H by gate F8. 5MHZ is the clock signal for Load Raster Control Latch K3 and Planet Control latch H5.

5MHZ

The Complementary 5 MHz Clock signal is hardware-generated at pin 6 of Clock latch C9. 5MHZ is the input signal for latch D5 in the Write Protection circuit. 5MHZ is the clock signal for Bit Map Shift Registers M9, P9, and R9. In the Multiply Clock, 5MHZ is the input signal for latches D8 and C8. In the Planet Control circuit, 5MHZ is the clock signal for latch D9. 5MHZ is gated with VASEG and LDRAST by gates N4 and P4 in the Line Buffer Address Controller circuit. In the Base RAM circuit, 5MHZ is gated with BASRAM by J5 to produce the write enable signal for Base RAM L5. In the Color Memory, 5MHZ is the clock signal for latches R5 and D5. It is also gated with COLORAM by gate J5 to produce the write enable signal for Color RAMs B11, C11, E11, and F11.

10MHZ

The 10 MHZ Clock signal is hardware-generated at pin 9 of Clock latch B8. The 10 MHZ signal is used to clock latches E8 of the Refresh circuit, D8 of the Multiply Clock circuit, and D5 of the Write Protection circuit. 10 MHZ is ANDed with 8H by gate F8 in the Horizontal Sync Chain to produce the clock signal for latch T4. In the Multiply Clock circuit, 10 MHZ is used by latch C8 to produce the CLRLDWE and PLS signals. In the Display Counter and Comparator circuit, 10 MHZ is gated with LBAINC by gate B9 to produce LATCHEN.

10MHZ

The Complementary 10 MHz Clock signal is hardware-generated at pin 8 of Clock latch B8. 10MHZ is the clock signal for latch C9 in the Refresh circuit; devices D9, E9, and F9 in the Horizontal Sync Chain; counters B6 and D6 in the Display Counter and Comparator; and latches A11 and D11 in the Color Memory. In addition, 10MHZ is gated with 20MHZ by gate B9 of the Display Counter and Comparator to produce the clock signal for flip-flop K4.

20MHZ

The 20 MHz Clock signal is hardware-generated by crystal clock Y1 in the Clock circuit. 20MHZ is the clock signal for latches B8 in the Clock and Multiply Clock circuits. In the Display Counter and Comparator, 20MHZ is gated with 10MHZ by gate B9 to produce the clock signal for flip-flop K4.

20MHZ

The Complementary 20 MHz Clock signal is hardware-generated at pin 4 of inverter A8 in the Clock circuit. 20MHZ is the clock signal for latches C8 and D8 of the Multiply Clock.

1V

Vertical Timing Signal 1 is hardware-generated at pin 14 of counter H8 in the Vertical Sync Chain. 1V and 2V are multiplexed by K8 and latched by M4 to produce VBLANK and VBLANK. Also, 1V is used by latch L8 to produce 1VDL. 1V is multiplexed with 128V, AB13, and AB6 by Bit Map Address Multiplexer L9.

2V

Vertical Timing Signal 2 is hardware-generated at pin 13 of counter H8 in the Vertical Sync Chain. 2V and 1V are multiplexed by K8 and latched by M4 to produce VBLANK and VBLANK. Also, 2V is used by latch L8 to produce 2VDL. 2V is multiplexed with 4H, AB7, and AB0 by Bit Map Address Multiplexer H9.

4V

Vertical Timing Signal 4 is hardware-generated at pin 12 of counter H8 in the Vertical Sync Chain. 4V and 8V are multiplexed by K8 and latched by M4 to produce VSYNC. Also, 4V is used by latch L8 to produce 4VDL. 4V is multiplexed with 8H, AB8, and AB1 by Bit Map Address Multiplexer H9.

8V

Vertical Timing Signal 8 is hardware-generated at pin 11 of counter H8 in the Vertical Sync Chain. 8V and 4V are multiplexed by K8 and latched by M4 to produce VSYNC. Also, 8V is used by latch L8 to produce 8VDL. 8V is multiplexed with 16H, AB9, and AB2 by Bit Map Address Multiplexer J9.

16V

Vertical Timing Signal 16 is hardware-generated at pin 14 of counter J8 in the Vertical Sync Chain. 16V and 32V are multiplexed by K8 and latched by M4 to produce IRQCK. Also, 16V is used by latch L8 to produce 16VDL. 16V is multiplexed with 32H, AB10, and AB3 by Bit Map Address Multiplexer J9. 16V is applied with AB1 to Base RAM decoder L7 to generate address bit 3 for Base RAM L5.

32V

Vertical Timing Signal 32 is hardware-generated at pin 13 of counter J8 in the Vertical Sync Chain. 32V and 16V are multiplexed by K8 and latched by M4 to produce IRQCK. Also, 32V is used by latch L8 to produce 32VDL. 32V is multiplexed with 64H, AB11, and AB4 by Bit Map Address Multiplexer K9.

64V

Vertical Timing Signal 64 is hardware-generated at pin 12 of counter J8 in the Vertical Sync Chain. 64V and 128V are multiplexed by K8 and latched by M4 to produce VPLA. 64V is applied through inverter A8 to produce 64V. 64V is multiplexed with 128H, AB12, and AB5 by Bit Map Address Multiplexer K9.

Liberator™ PCB Signal Name Descriptions

Description of Liberator PCB Signal Names (continued)

$\overline{64V}$

Complementary Vertical Timing Signal 64 is hardware-generated at pin 8 of inverter A8 in the Vertical Sync Chain. $\overline{64V}$ is used by latch L8 in the Vertical Sync Chain.

128V

Vertical Timing Signal 128 is hardware-generated at pin 11 of counter J8 in the Vertical Sync Chain. 128V and 64V are multiplexed by K8 and latched by M4 to produce $\overline{VPLA}$. 128V is the clock 1 signal for counter J11 of the Power-On Reset circuit. 128V is also multiplexed with 1V, AB13, and AB6 by Bit Map Address Multiplexer L9. 128V is applied with AB3 to Base RAM decoder L7 to generate address bit 4 for Base RAM L5.

1VDL

Delayed Vertical Timing Signal 1 is hardware-generated at pin 5 of latch L8 in the Vertical Sync Chain. 1VDL is derived from 1V after a delay by $\overline{HBLANK}$*. 1VDL is address bit 5 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 0 for Latitude Scalers P6 and N6.

2VDL

Delayed Vertical Timing Signal 2 is hardware-generated at pin 15 of latch L8 in the Vertical Sync Chain. 2VDL is derived from 2V after a delay by $\overline{HBLANK}$*. 2VDL is address bit 6 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 1 for Latitude Scalers P6 and N6.

4VDL

Delayed Vertical Timing Signal 4 is hardware-generated at pin 9 of latch L8 in the Vertical Sync Chain. 4VDL is derived from 4V after a delay by $\overline{HBLANK}$*. 4VDL is address bit 7 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 2 for Latitude Scalers P6 and N6.

8VDL

Delayed Vertical Timing Signal 8 is hardware-generated at pin 6 of latch L8 in the Vertical Sync Chain. 8VDL is derived from 8V after a delay by $\overline{HBLANK}$*. 8VDL is address bit 8 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 3 for Latitude Scalers P6 and N6.

16VDL

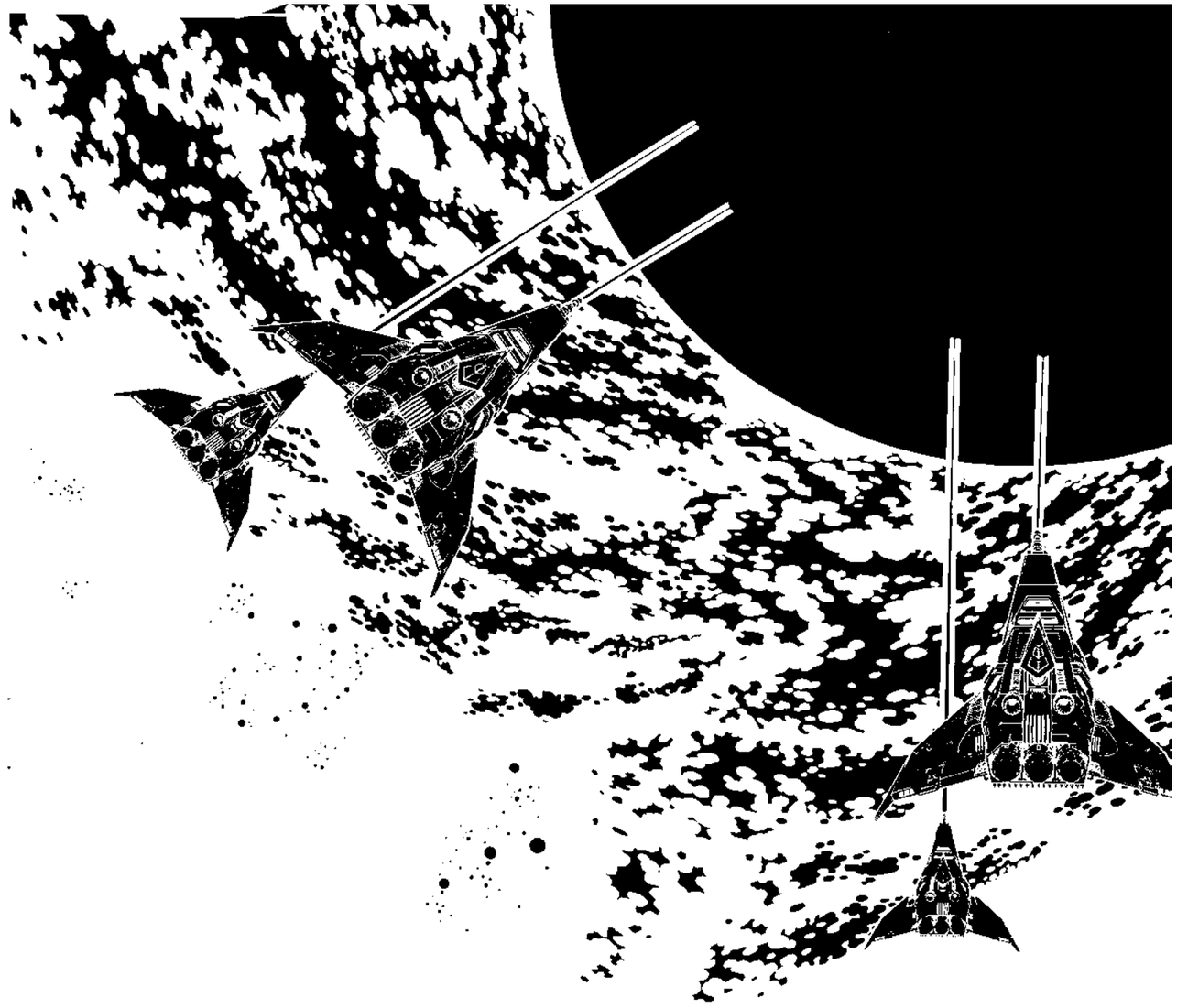
Delayed Vertical Timing Signal 16 is hardware-generated at pin 2 of latch L8 in the Vertical Sync Chain. 16VDL is derived from 16V after a delay by $\overline{HBLANK}$*. 16VDL is address bit 9 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 4 for Latitude Scalers P6 and N6.

32VDL

Delayed Vertical Timing Signal 32 is hardware-generated at pin 19 of latch L8 in the Vertical Sync Chain. 32VDL is derived from 32V after a delay by $\overline{HBLANK}$*. 32VDL is address bit 10 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 5 for Latitude Scalers P6 and N6.

$\overline{64VDL}$

Delayed Vertical Timing Signal 64 is hardware-generated at pin 12 of latch L8 in the Vertical Sync Chain. $\overline{64VDL}$ is derived from $\overline{64V}$ after a delay by $\overline{HBLANK}$*. $\overline{64VDL}$ is address bit 11 for Planet Picture ROMs P8, M/N8, T8, and R/S8; and it is address bit 6 for Latitude Scalers P6 and N6.



Liberator™ PCB Signal Name Descriptions

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Liberator™ Troubleshooting with the CAT Box

Table of Contents

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the Φ0 and Φ2 test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{\text{WDDIS}}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{\text{W}}$
11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

B. Checking the Address Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: READ
3. Key in the address pattern given in Table 1 *(use AAAA to start)* with the CAT Box keyboard.
4. Set R/W MODE to STATIC.
5. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
6. Repeat parts 2-c through 5 using address *5555* in part 3.

Table 1 Address Lines

LOGIC STATE FOR ADDRESS *AAAA*	IC-PIN	LOGIC STATE FOR ADDRESS *5555*
1	T2-3	0
0	T2-2	1
1	B1-11	0
0	B1-13	1
1	B1-9	0
0	B1-7	1
1	B1-5	0
0	B1-3	1
1	E1-7	0
0	E1-9	1
1	E1-5	0
0	E1-3	1
1	E1-12	0
0	E1-14	1
1	E1-16	0
0	E1-18	1

C. Checking the Data Lines

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{\text{W}}$ MODE: (OFF)
    c. R/$\overline{\text{W}}$: WRITE
3. Key in address *0000* with the keyboard.
4. Press DATA SET. Key in data *AA* with the keyboard.
5. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
6. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
7. Repeat parts 4 through 6 using data *55* in part 4.

Table 2 Data Lines

LOGIC STATE FOR DATA *AA*	IC-PIN	LOGIC STATE FOR DATA *55*
1	E2-11	0
0	E2-12	1
1	E2-13	0
0	E2-14	1
1	E2-15	0
0	E2-16	1
1	E2-17	0
0	E2-18	1
1	E2-9	0
0	E2-8	1
1	E2-7	0
0	E2-6	1
1	E2-5	0
0	E2-4	1
1	E2-3	0
0	E2-2	1

D. Checking the RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. DBUS SOURCE: ADDR
    b. BYTES:1024
    c. R/$\overline{\text{W}}$ MODE: (OFF)
    d. R/$\overline{\text{W}}$: WRITE
3. Enter address *0003* with the keyboard.

NOTE

Addresses *0000*, *0001*, and *0002* are special RAM locations for bit mode operation that cannot be verified by this RAM test.

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Liberator™ PCB Troubleshooting

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4. Set the CAT Box switches as indicated:
   a. R/$\overline{W}$ MODE to PULSE and back to (OFF)
   b. R/$\overline{W}$ to READ
   c. R/$\overline{W}$ MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat parts 2-d through 4 using addresses *0400, 0800, 0C00, 1000, 1400, 1800, 1C00, 2000, 2400, 2800, 2C00, 3000, 3400, 3800,* and *3C00.*
7. Repeat this test with DBUS SOURCE set to $\overline{ADDR}$.

E. Checking the Custom Audio I/O Chips

NOTE

Liberator has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:
- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

ADDRESS	DATA	TEST RESULTS
780F	*00*	
780F	*03*	
7800	*55*	
7801	*AF*	Custom Audio I/O Chip B3 channel 1 produces pure tone.
7801	*00*	Custom Audio I/O Chip B3 channel 1 off.
7802	*55*	
7803	*AF*	Custom Audio I/O Chip B3 channel 2 produces pure tone.
7803	*00*	Custom Audio I/O Chip B3 channel 2 off.
700F	*00*	
700F	*03*	
7000	*55*	
7001	*AF*	Custom Audio I/O Chip C/D3 channel 1 produces pure tone.
7001	*00*	Custom Audio I/O Chip C/D3 channel 1 off.
7002	*55*	
7003	*AF*	Custom Audio I/O Chip C/D3 channel 2 produces pure tone.
7003	*00*	Custom Audio I/O Chip C/D3 channel 2 off.

F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
3. Enter address *6C04* with the keyboard.
4. Press DATA SET and enter data *00* with the keyboard.
5. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{CTRLD}$ signal is now set to the low state.
6. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: READ
7. For each address listed in Table 4, do the following:
   a. Set R/$\overline{W}$ MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/$\overline{W}$ MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address and check the test result.
8. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{W}$: WRITE
   c. R/$\overline{W}$ MODE: (OFF)
9. Enter address *6C02* with the keyboard.
10. Press DATA SET and enter data *00* with the keyboard.
11. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{TBSWP}$ signal is now set to the low state.
12. Enter address *6C04* with the keyboard.
13. Press DATA SET and enter data *01* with the keyboard.
14. Set R/$\overline{W}$ MODE to PULSE and back to (OFF). The $\overline{CTRLD}$ signal is now set to the high state.
15. Set R/$\overline{W}$ to READ.
16. Set R/$\overline{W}$ MODE to (OFF).
17. Enter address *5000* with the keyboard.
18. Set R/$\overline{W}$ MODE to STATIC and check for the result shown in Table 5.

Table 4 Player and DIP Switch Inputs (with $\overline{CTRLD}$ Low)

ADDRESS	INPUT SWITCH	TEST RESULTS
5000	Slam, Right coin switch, Left coin switch, Self-Test switch, Auxillary coin switch.	DATA display changes when any coin or self-test switch is activated.
5001	FIRE 1, SHIELD 1, FIRE 2, SHIELD 2, START 1, START 2	DATA display changes when any of these switches is activated. (Note that display changes also without activating a switch because of VBLANK).

Table 5 TRAK-BALL™ Inputs (with $\overline{CTRLD}$ High and $\overline{TBSWP}$ Low)

ADDRESS	TRAK-BALL	TEST RESULT
5000	TRAK-BALL	Data display changes when TRAK-BALL is rolled.

G. Checking the LED and Coin Counter Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{W}$: WRITE
   d. R/$\overline{W}$ MODE: (OFF)

CAUTION

If you write ON data to activate a solenoid, *deactivate the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

3. For each address listed in Table 6, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter data *00* with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter data *FF* with the keyboard.
      - Set R/$\overline{W}$ MODE to STATIC and back to (OFF).

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Liberator™ PCB Troubleshooting

Table 6 LED and Coin Counter Outputs

ADDRESS	DATA (0)	(FF)	OUTPUT DEVICE
6C00	*ON*	*OFF*	Player 1 LED
6C01	*ON*	*OFF*	Player 2 LED
6C04	*LOW*	*HIGH*	$\overline{CTRLD}$
6C05	*ON*	*OFF*	Coin Counter Right
6C06	*ON*	*OFF*	Coin Counter Left
6C07	*ON*	*OFF*	PLANET

Troubleshooting with Signature Analysis

A. Checking the Address Lines and Address Decoders

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{W}$: WRITE
   d. R/$\overline{W}$ MODE: (OFF)
3. Enter address *0000* with the keyboard.
4. Press DATA SET and enter data *08* with the keyboard.
5. Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
6. Enter address *0001* with the keyboard.
7. Press DATA SET and enter data *00* with the keyboard.
8. Set R/$\overline{W}$ MODE to STATIC and back to (OFF).
9. Connect the three BNC-to-EZ clip cables supplied with the CAT Box to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks of the CAT Box.
10. Connect the three black EZ clips to a game PCB ground test point.
11. Ground pin 4 of IC H4 (the DISDAT signal) on the game PCB.
12. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. TESTER SELF-TEST: OFF
    c. PULSE MODE: LATCHED
    d. START: Negative-going edge trigger
    e. STOP: Negative-going edge trigger
    f. CLOCK: Negative-going edge trigger
13. Press TESTER RESET on the CAT Box.
14. Connect the CAT Box Signature Analysis probe tips as indicated:
    a. START: Pin 3 of IC T2
    b. STOP: Pin 3 of IC T2
    c. CLOCK: Φ2 test point
15. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show *0000*. Now connect the DATA PROBE to a +5V test point. The ADDRESS/SIGNATURE display should show *0001*.
16. Probe the IC-pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 7 Address Bus Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
E1-18	AB0	*UUUU*
E1-16	AB1	*5555*
E1-14	AB2	*CCCC*
E1-12	AB3	*7F7F*
E1-3	AB4	*5H21*
E1-5	AB5	*0AFA*
E1-9	AB6	*UPFH*
E1-7	AB7	*52F8*
B1-3	AB8	*HC89*
B1-5	AB9	*2H70*
B1-7	AB10	*HPP0*
B1-9	AB11	*1293*
B1-13	AB12	*HAP7*
B11-11	AB13	*3C96*
T2-2	A14	*3827*
R2-3	A15	*755U*

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

17. Probe the IC-pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 8 Decoder Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
E4-0	$\overline{BITMD}$	*4001*
E4-8	BITMD	*4000*
E4-5	YCOORD	*8001*
E4-4	XCOORD	*0000*
E4-12	$\overline{EARD}$	*6FHH*
E4-11	$\overline{IN0}$	*57HH*
E4-10		*96F8*
E4-9	$\overline{IOS}$	*546U*
E4-4	$\overline{RAM}$	*5FU8*
T3-12	$\overline{ROM0}$	*CA11*
T3-11	$\overline{ROM1}$	*H759*
T3-10	$\overline{ROM2}$	*A3UH*
T3-9	$\overline{ROM3}$	*AA6A*
H4-8	$\overline{ROM}$	*755U*
T2-12	$\overline{ROM4}$	*A711*
T2-11	$\overline{ROM5}$	*54F5*
P3-8	$\overline{ROM6}$	*P255*

B. Checking the Planet-Generating Circuitry

1. Perform steps 1 through 7 of the CAT Box preliminary set-up.
2. Connect the CAT Box Signature Analysis probe tips where indicated:
   a. START: Pin 11 of IC E9
   b. STOP: Pin 11 of IC E9
   c. CLOCK: Pin 8 of IC B8
3. Connect the ground clips of the CAT Box Signature Analysis and DATA probes to a game PCB ground test point.
4. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: UNLATCHED
   d. START: Positive-going edge trigger
   e. STOP: Positive-going edge trigger
   f. CLOCK: Positive-going edge trigger
5. Turn on the game and the CAT Box.
6. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *A70F*.
7. Test the signatures designated by (XXXX)1 printed in color on the schematic diagrams of the game PCB. To test for a signature, use the CAT Box DATA PROBE to probe the appropriate location on the game PCB. Then check the ADDRESS/SIGNATURE display for the appropriate signature.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

8. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated by (XXXX)1↓ on the schematics.
9. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 11 of IC F9
   b. STOP: Pin 11 of IC F9
10. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *1308*.
11. Set the CAT Box CLOCK switch for a positive-going edge trigger and test the signatures designated on the schematics by (XXXX)2.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

12. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 11 of IC J8
    b. STOP: Pin 11 of IC J8
13. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *H57U*.
14. Test the signatures designated on the schematics by (XXXX)3.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

15. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)3↓.
16. Remove the electrical power from the game and the CAT Box.
17. Connect the CAT Box flex cable to the game PCB edge test connector and connect the game PCB PSIG1 test point to ground.
18. Apply power to the game and the CAT Box.

Continued on back of sheet

Liberator™ PCB Troubleshooting

19. Set the CAT Box switches as indicated:
    a. TESTER MODE: R/$\overline{W}$
    b. BYTES: 1
    c. R/$\overline{W}$: WRITE
    d. R/$\overline{W}$ MODE: (OFF)
20. Press TESTER RESET.
21. Enter address *6800* with the keyboard.
22. Press DATA SET and enter data *00* with the keyboard.
23. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
24. Enter address *6C07* with the keyboard and repeat steps 22 and 23.
25. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. START: Negative-going edge trigger
    c. STOP: Negative-going edge trigger
    d. CLOCK: Positive-going edge trigger
26. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 12 of IC L8
    b. STOP: Pin 12 of IC L8
    c. CLOCK: Pin 10 of IC A8
27. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
28. Test the signatures designated on the schematics by (XXXX)4.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

29. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)4↓.
30. Set TESTER MODE to R/$\overline{W}$ and enter address *6800* with the keyboard.
31. Press DATA SET and enter data *7F* with the keyboard.
32. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
33. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. START: Positive-going edge trigger
    c. STOP: Negative-going edge trigger
    d. CLOCK: Positive-going edge trigger
34. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 2 of IC M4
    b. STOP: Pin 2 of IC M4
35. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
36. Test the signatures designated on the schematics by (XXXX)5.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

37. Connect pin 8 of IC P4 and connect test point $\overline{PSIG2}$ to a game PCB ground test point.
38. Set TESTER MODE to R/$\overline{W}$ and enter address *6000* with the keyboard.
39. Press DATA SET and enter data *00* with the keyboard.
40. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
41. Repeat steps 38 through 40 for addresses *6001, 6002, 6003, 6004, 6005, 6006, 6007, 6008, 6009, 600A, 600B, 600C, 600D, 600E, 600F,* and *6800*.
42. Set TESTER MODE to SIG.
43. Connect the CAT Box CLOCK probe tip to pin 8 of IC C8.
44. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for *FP96*.
44. Test the signatures designated on the schematics by (XXXX)6A.

NOTE

To avoid faulty readings while performing these troubleshooting tests, take care **NOT** to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

45. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)6A↓.
46. Remove the ground connection from pin 8 of IC P4 and from test point $\overline{PSIG2}$.
47. Connect the CAT Box CLOCK probe tip to pin 14 of IC E9 and set the CLOCK switch for a positive-going edge trigger.
48. Test the signatures designated on the schematics by (XXXX)6B.

Troubleshooting with Checksums

NOTE

This procedure can only be done with those CAT Boxes equipped with a Checksum Switch.

CAUTION

While testing with checksums, adding 100 pF capacitors to A14 and A15 may be necessary.

1. Perform the CAT Box preliminay set-up.
2. Set the CAT Box switches as indicated:
    a. BYTES: 256
    b. DBUS SOURCE: DATA
    c. R/$\overline{W}$ MODE: OFF
    d. CHECKSUM SWITCH: ON
3. Key in the address pattern given in Table 9 *(use 8000 to start).*
4. Set the R/$\overline{W}$ MODE switch to PULSE and then back to (OFF).
5. Check the CAT Box ADDRESS/SIGNATURE display for the appropriate checksum.
6. Repeat parts 3 through 5 for each address listed in Table 9.

Table 9 ROM Checksums

ADDRESS	ROM TESTED	CHECKSUM
8000	ROM0	*2D29*
9000	ROM1	*EFDD*
A000	ROM2	*8265*
B000	ROM3	*17AB*
C000	ROM4	*E41F*
D000	ROM5	*55A7*
E000	ROM6	*BBE7*

Troubleshooting the Watchdog Circuit

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

$\overline{RESET}$ is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing $\overline{RESET}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{RESET}$ signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator. To aid in troubleshooting, the $\overline{WDDIS}$ test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition. □

Liberator™ PCB Troubleshooting

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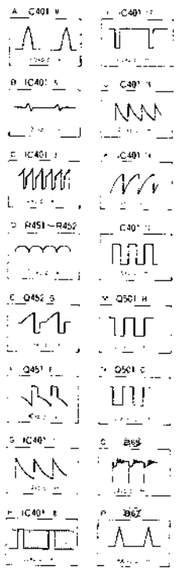
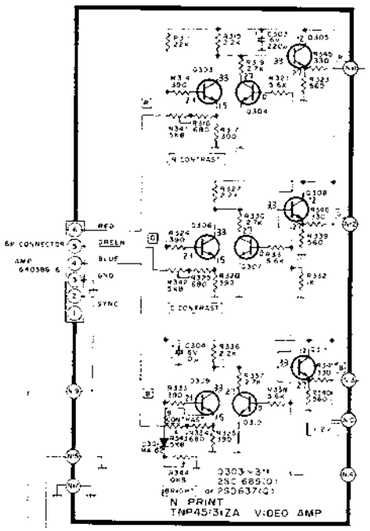
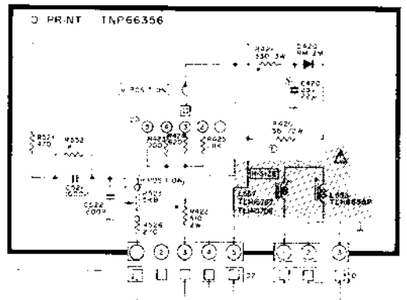
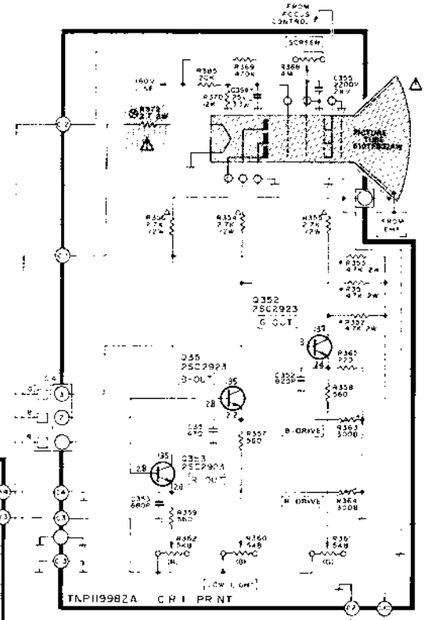
1st Printing

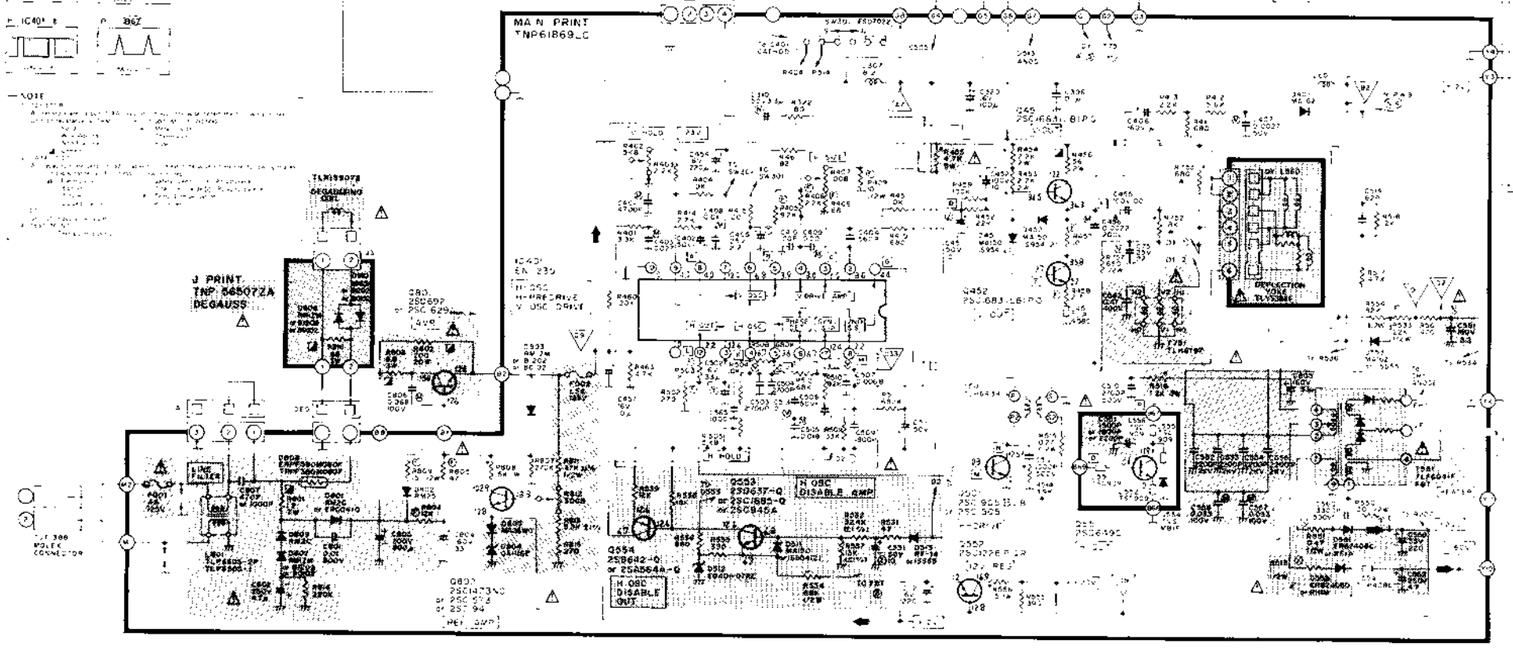
Waveform











WARNING

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

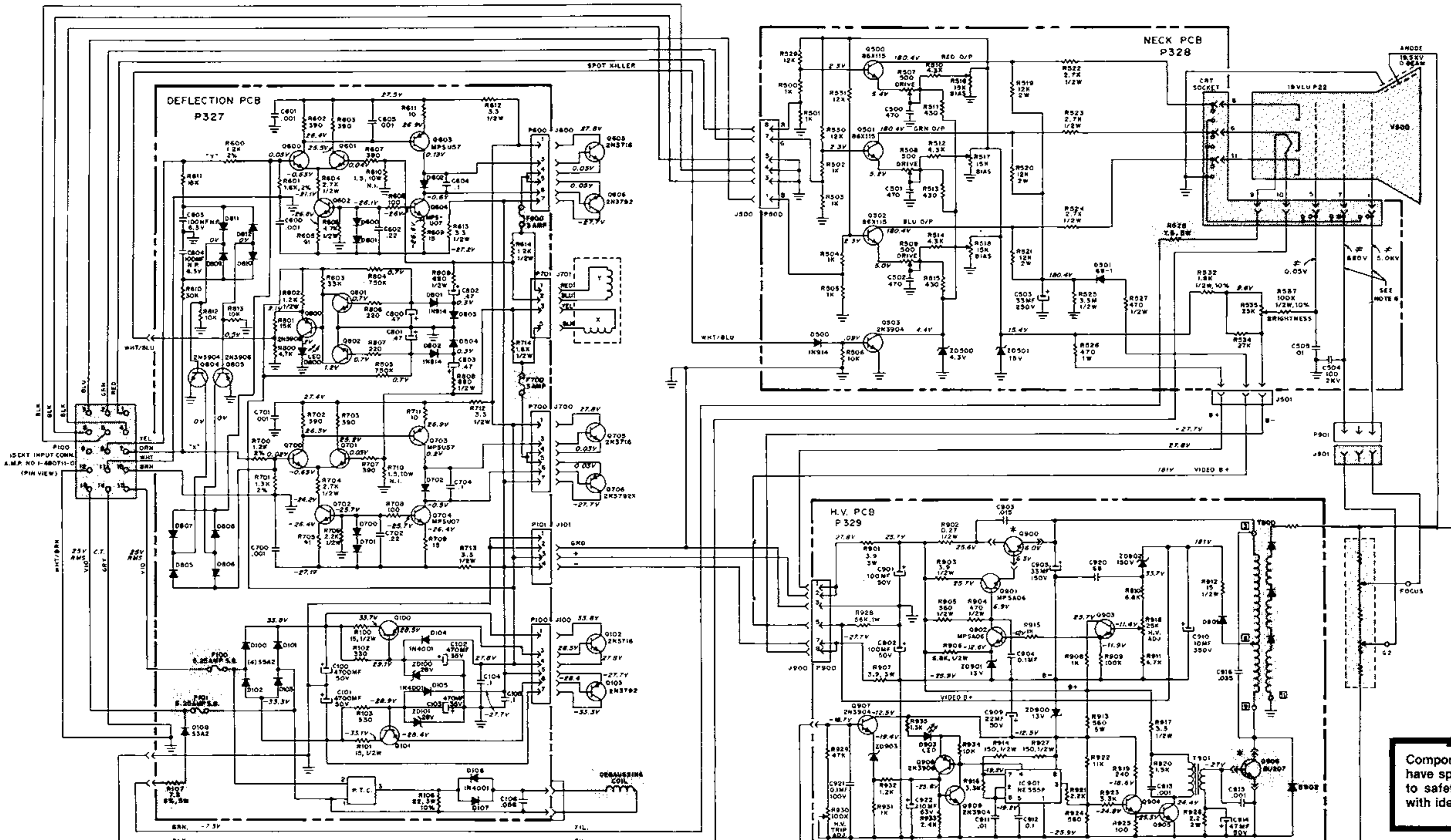
ATARI®

Matsushita Color Raster Display Schematic

A Warner Communications Company

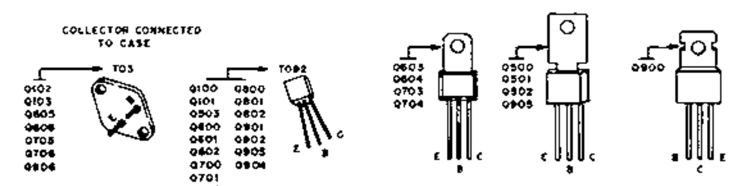
SP-209 Sheet 14A

1st Printing



⚠ WARNING ⚠

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.



GENERAL NOTES:

1. RESISTANCE VALUES IN OHMS 1/4 WATT, 5% UNLESS OTHERWISE NOTED. K=1,000, M=1,000,000
2. CAPACITANCE VALUE OF 1 OR LESS IN MICROFARADS, ABOVE 1 IN PICOFARADS UNLESS OTHERWISE NOTED.
3. * Q900 AND Q906 ARE NOT ON H.V.P.C.B.
4. ALL D.C VOLTAGES 10% MEASURED FROM POINT INDICATED TO GROUND USING A HIGH IMPEDANCE METER. VOLTAGES ARE MEASURED WITH NO SIGNAL INPUT AND CONTROLS ARE IN A NORMAL OPERATING POSITION
5. CIRCLED NUMBERS INDICATE LOCATION OF WAVE-FORM READING.
6. USE A 1,000:1 PROBE WHEN MEASURING SCREEN OR FOCUS VOLTAGE.
7. ≠ VOLTAGES VARY WITH CONTROL SETTINGS.

ATARI®

Wells-Gardner Color Raster Display Schematic

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SP-209 Sheet 14B

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Electrohome 19-Inch Color Raster-Scan Video Display Schematic Diagram

Schematic Notes

Unless otherwise specified
Resistance: (Ω) (K→KΩ, M→MΩ), 1/4 (W) carbon resistor
Capacitance: 1 or higher→ (pF), less than 1→ (μF)
working voltage→ 50 (V)
ceramic capacitor
Inductance: (μH)
Electrolytic Cap: Capacitance Value (μF)/working voltage (V),
NP → non-polar (or bipolar) electrolytic cap.
Refer to the parts list for additional component information.

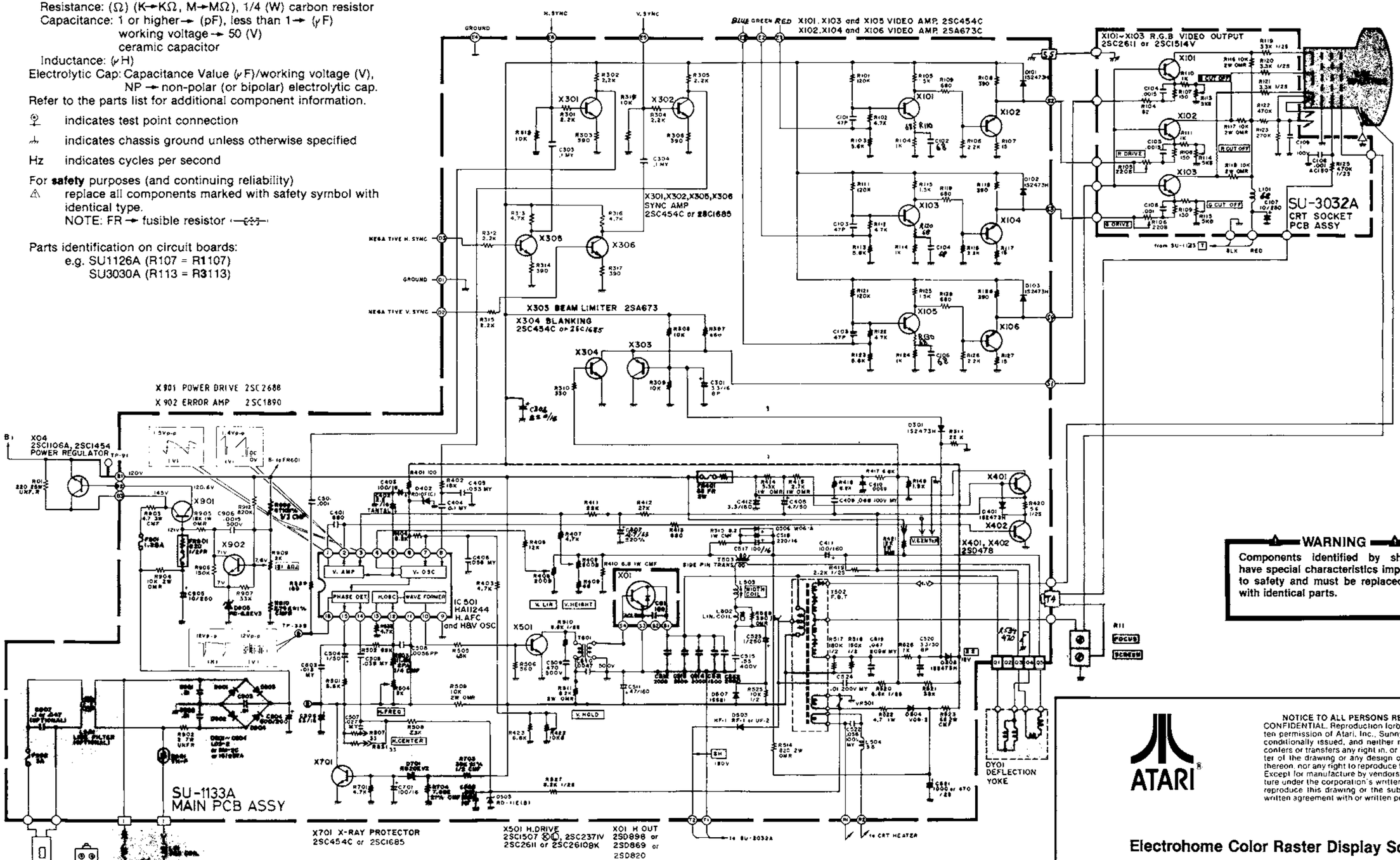
⏚ indicates test point connection

⏚ indicates chassis ground unless otherwise specified

Hz indicates cycles per second

For **safety** purposes (and continuing reliability)
⚠ replace all components marked with safety symbol with identical type.
NOTE: FR → fusible resistor

Parts identification on circuit boards:
e.g. SU1126A (R107 = R1107)
SU3030A (R113 = R3113)



⚠ WARNING ⚠

Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Electrohome Color Raster Display Schematic